TESIS – EE142599

SISTEM PENGISIAN BATERAI NIRKABEL DENGAN PANEL SURYA MENGGUNAKAN METODE FUZZY

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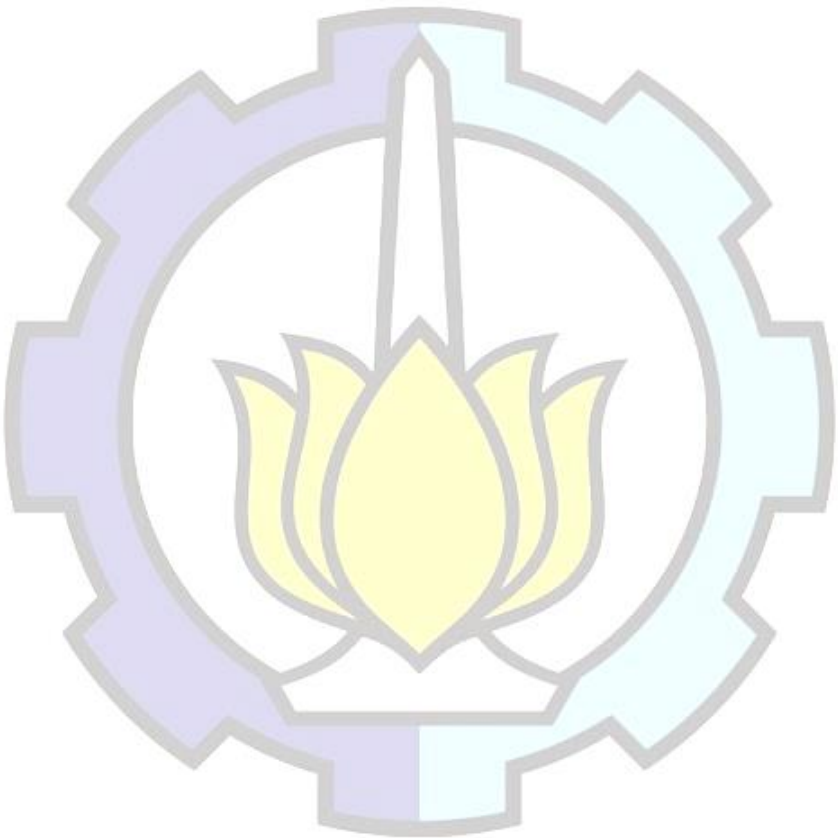
SURABAYA
2020



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LEMBAR PENGESAHAN TESIS

Tesis disusun untuk memenuhi salah satu syarat memperoleh gelar
Magister Teknik (M.T.)
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Oleh
ALFARID HENDRO YUWONO
NRP: 07111650042001

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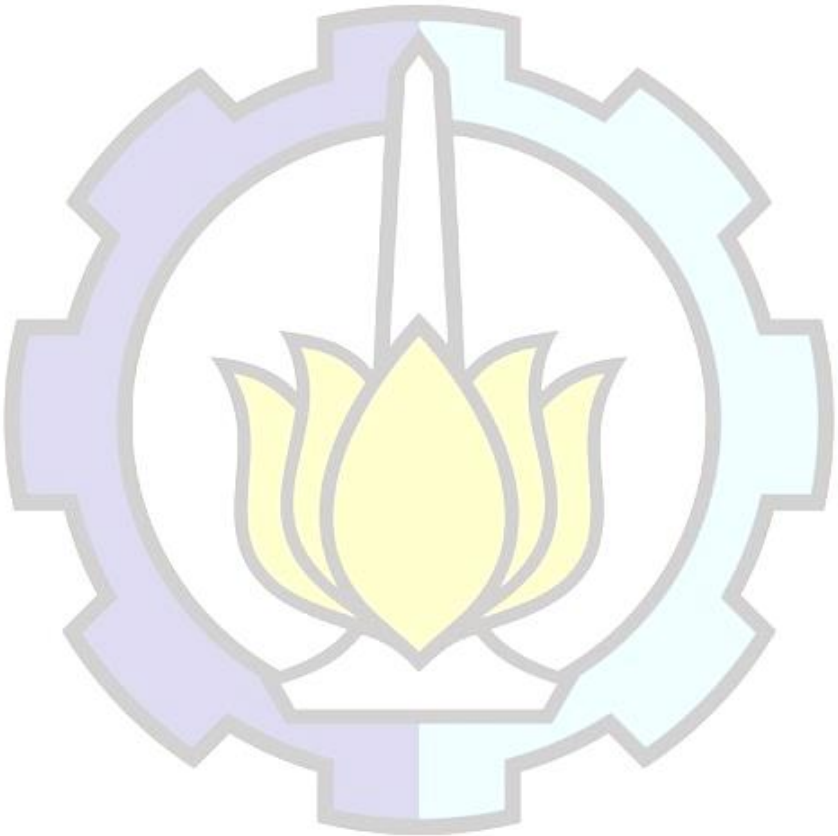
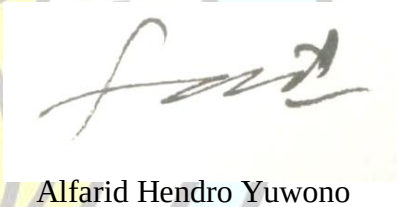


PERNYATAAN KEASLIAN TESIS

Dengan ini saya menyatakan bahwa isi keseluruhan Tesis saya dengan judul "**SISTEM PENGISIAN BATERAI NIRKABEL DENGAN PANEL SURYA MENGGUNAKAN METODE FUZZY**" adalah benar-benar hasil karya intelektual mandiri, diselesaikan tanpa menggunakan bahan-bahan yang tidak diijinkan dan bukan merupakan karya pihak lain yang saya akui sebagai karya sendiri.

Semua referensi yang dikutip maupun dirujuk telah ditulis secara lengkap pada daftar pustaka. Apabila ternyata pernyataan ini tidak benar, saya bersedia menerima sanksi sesuai peraturan yang berlaku.

Surabaya, 26 Desember 2019



Alfarid Hendro Yuwono

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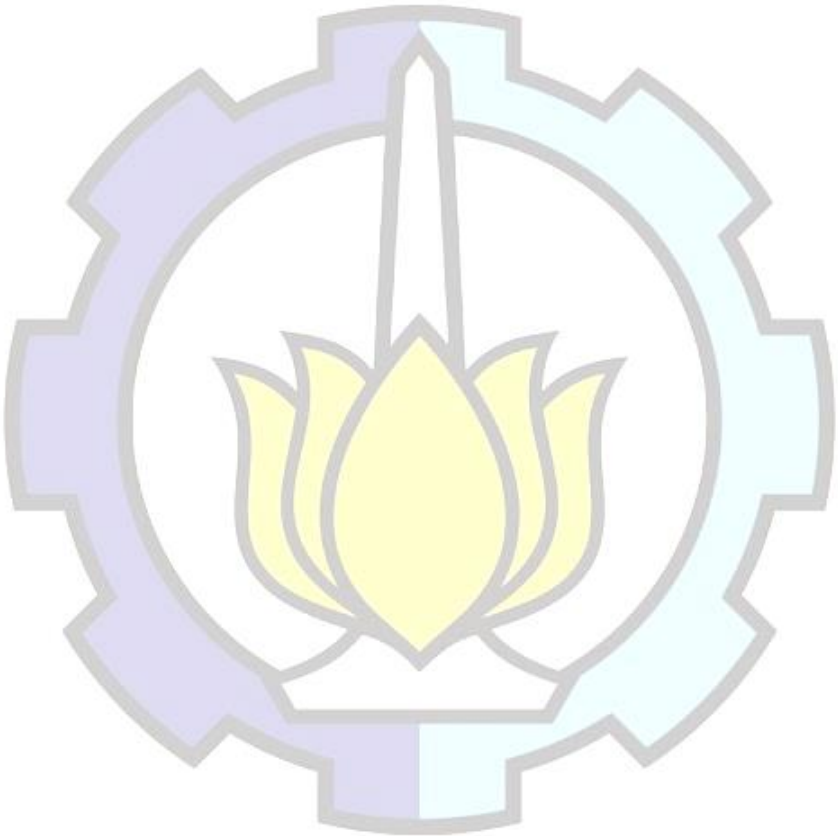

SISTEM PENGISIAN BATERAI NIRKABEL DENGAN PANEL SURYA MENGGUNAKAN METODE FUZZY

Nama mahasiswa : Alfarid Hendro Yuwono
NRP : 07111650042001
Pembimbing : 1. Dr. Muhammad Rivai, S.T., M.T.
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ABSTRAK

Perkembangan teknologi yang cepat mengarah pada pertumbuhan perangkat elektronik yang ditenagai oleh baterai. Ini membutuhkan sistem pengisian baterai yang sederhana, cepat dan aman. Dalam studi ini, kami telah merancang dan merealisasikan sistem pengisian baterai nirkabel yang dipasok oleh panel surya menggunakan metode kontrol fuzzy. Sistem ini dilengkapi dengan pelacakan matahari untuk menghasilkan daya listrik yang optimal. Selanjutnya, sistem kontrol fuzzy diterapkan untuk menentukan jumlah tegangan pengisian dengan memperhitungkan suhu baterai. Hasil percobaan menunjukkan bahwa sistem pelacakan matahari dapat meningkatkan kinerja panel surya. Sistem selalu mendeteksi suhu baterai dan akan mengurangi nilai tegangan selama proses pengisian saat suhu meningkat. Sistem pengisian baterai ini juga akan secara otomatis mengurangi tegangan pengisian ketika tegangan baterai mendekati nilai maksimum. Sistem pengisian wireless ini menggunakan panel surya 100 WP dengan sistem tracking matahari, ditambah dengan sistem pembangkit sinyal gelombang sinus frekuensi 90 kHz dan 2 buah kumparan sebagai sistem transmisi energi berbasis wireless charging. Sistem ini dapat digunakan sebagai sistem pengisian baterai cepat tanpa mempengaruhi masa pakai baterai.

Kata kunci: *Fuzzy logic, panel surya, pengisian baterai nirkabel*

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WIRELESS BATTERY CHARGING SYSTEM WITH SOLAR PANEL USING FUZZY METHOD

By : Alfarid Hendro Yuwono
Student Identity Number : 071116500042001
Supervisor(s) : 1. Dr. Muhammad Rivai, S.T., M.T.
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ABSTRACT

Rapid technological development leads to the growth of electronic devices powered by batteries. This requires a simple, fast and safe battery charging system. In this study, we have designed and realized a wireless battery charging system supplied by solar panel using the fuzzy control method. This system is equipped with solar tracking to produce optimal electric power. Furthermore, fuzzy control system is applied to determine the amount of charging voltage by taking into account the temperature of the battery. The experimental results show that the solar tracking system can improve the performance of solar panel. The system always detects the temperature of the battery and will reduce the voltage value during the charging process as the temperature increases. This battery charging system will also automatically decrease the charging voltage when the battery voltage approaches the maximum value. This wireless charging system uses a 100 WP solar panel with a solar tracking system, coupled with a 90 kHz sine wave signal generator system and 2 coils as a wireless charging energy transmission system. This system can be used as a fast battery charging system without affecting the battery lifetime.

Keywords: *Fuzzy logic, solar panels, wireless battery charging*

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Penulis ucapkan banyak terima kasih kepada semua pihak sehingga dapat membantu penulis dalam menyelesaikan tesis. Semoga Allah SWT. Membalas

kebaikan kalian semua dengan sebaik-baiknya balasan. Aamiin yaa robbal'aalamiin.

Surabaya, 26 Desember 2019

Penulis

DAFTAR ISI

DAFTAR GAMBAR

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DAFTAR TABEL

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BAB 1
PENDAHULUAN

1.1 Latar Belakang

Semakin berkembangnya teknologi maka semakin banyak kebutuhan akan teknologi seperti Handphone, laptop, mobile robot, dll. Kebutuhan ini kemudian diikuti oleh kebutuhan akan internet, pengisian listrik, dan informasi.

Penelitian mengenai transfer daya nirkabel terus dilakukan dan digunakan dalam berbagai bidang. Pemanfaatan dari transfer daya nirkabel cukup beragam, mulai dari bidang kedokteran hingga industri. Pada bidang kedokteran atau medis, transfer daya nirkabel digunakan untuk mensuplai daya perangkat-perangkat elektronik implant pada tubuh seorang pasien [1]. Selain itu, pada industri otomotif juga mulai mengembangkan sistem transfer daya nirkabel untuk mengisi daya mobil listrik produksi mereka [2], [3].

Salah satu permasalahan pada sistem transfer daya nirkabel yang telah diterapkan adalah lamanya waktu yang dibutuhkan untuk melakukan charging pada suatu perangkat elektronik [4]. Hal ini dikarenakan daya yang ditransfer oleh sistem cenderung konstan tanpa memdulikan kondisi daya yang tersedia pada baterai yang diisi.

Wireless power transfer atau transfer daya nirkabel menggunakan medan elektromagnetik untuk mentransfer energi antara dua benda. Hal ini biasanya dilakukan dengan menggunakan metode induktif. Energi dikirim melalui kumparan ke perangkat listrik, yang kemudian dapat menggunakan energi itu untuk mengisi baterai atau menjalankan perangkat [5].

Panel surya merupakan solusi alternatif sebagai sumber energi listrik terbaru yang hemat dan tidak menimbulkan dampak polusi. Penggunaan panel surya masih dikatakan sedikit sehingga masih jarang yang menggunakannya. Kebutuhan kontrol untuk panel surya juga membutuhkan alat yang kompleks agar panel surya dapat bekerja optimal dan menghasilkan energi listrik yang cukup besar.

Maka digunakan metode pengisian aki nirkabel dengan panel surya dengan menggunakan metode fuzzy logic yang lebih praktis dan simple saat pengisian baterai. Sistem ini menggabungkan sistem yang pernah ada menjadi lebih kompleks, sehingga daya yang dihasilkan dari panel surya menjadi lebih maksimal serta sistem pengisian aki yang praktis tanpa harus memasang kabel, simple, mudah, cepat, dan memiliki tingkat efisiensi yang tinggi.

1.2 Rumusan Masalah

1. Bagaimana mendapatkan energi matahari secara maksimal
2. Bagaimana cara agar dapat dilakukan pengisian secara praktis
3. Sistem yang bisa melakukan pengisain secara cepat dan aman

1.3 Tujuan

1. Membuat sistem pelacakan berbasis sensor cahaya
2. Rancang bangun pengisian secara nirkabel
3. Implementasi metode kontrol oleh fuzzy logic yang pemberian daya dipengaruhi oleh suhu, arus dan tegangan.

1.4 Batasan Masalah

Batasan masalah pada penelitian ini adalah antara lain adalah:

1. Sistem pengisian aki nirkabel menggunakan media udara dengan suhu kamar dan jarak tertentu
2. Menggunakan panel surya 100 WP

1.5 Kontribusi

Kontribusi yang diharapkan dari hasil penelitian thesis antara lain:

1. Menghasilkan sistem pengisian aki dengan sumber energi listrik yang berasal dari panel surya.
2. Menghasilkan sistem pengisian aki secara nirkabel.
3. Menghasilkan pengisian aki yang adaptif dengan metode fuzzy sehingga mempercepat proses pengisian aki.

BAB 2
SISTEM PENGISIAN BATERAI NIRKABEL DENGAN PANEL SURYA MENGGUNAKAN METODE FUZZY

Bab ini mengemukakan penelitian terkait dengan aplikasi rangkaian sistem pengisi baterai nirkabel dengan panel surya menggunakan metode fuzzy serta perangkat-perangkat yang digunakan pada penelitian ini sebagai bahan referensi.

2.1 Kajian Penelitian Terkait

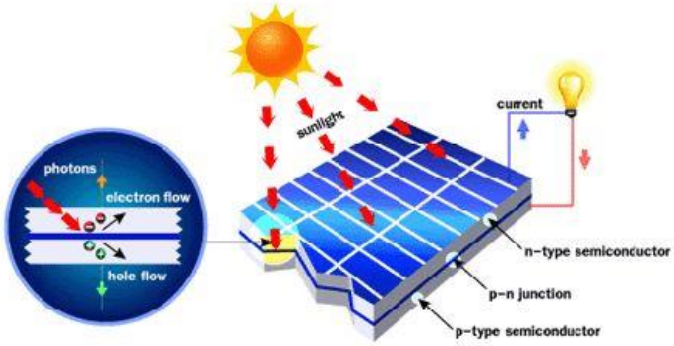
Beberapa penelitian yang telah dilakukan diantaranya adalah rancang bangun sistem pengisian baterai nirkabel menggunakan mikrokontroler Teensy[6]. Implementasi hidung elektronik (*e-nose*) pada *mobile robot omnidirectional* menggunakan susunan sensor gas untuk mengidentifikasi pola dari respon masing-masing sensor gas terhadap bensin dan alkohol [7]. Pengimplementasian metode kendali *fuzzy* pada *mobile robot* untuk mencari sumber gas berbasis sensor gas MQ-4 [8].

2.2 Panel Surya

Sel surya atau yang disebut juga Fotovoltaik adalah piranti semikonduktor yang dapat mengubah energi matahari secara langsung menjadi energi listrik DC (arus searah) dengan menggunakan kristal silicon yang tipis. Sel-sel silikon itu dipasang dengan posisi sejajar/seri dalam sebuah panel yang terbuat dari alumunium atau baja anti karat dan dilindungi oleh kaca atau plastik.

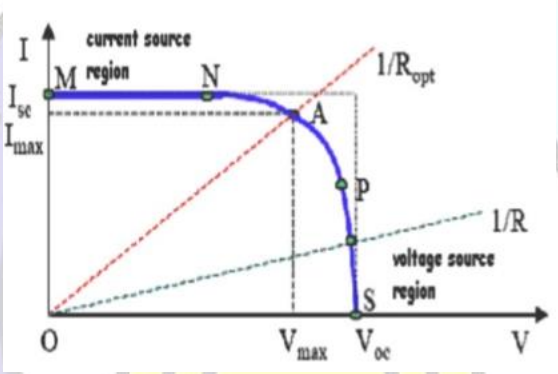
Sigalingging menyatakan bahwa pada umumnya sel surya memiliki ketebalan minimum 0.3 mm, yang terbuat dari irisan bahan semikonduktor dengan kutub Positip dan Negatif [9]. Wasito menyatakan bahwa dioda listrik surya / sel surya merupakan suatu dioda yang dapat mengubah energi surya / matahari secara langsung menjadi energi listrik (berdasarkan sifat foto elektrik yang ada pada setengah penghantar)[10]. Bila sel-sel itu terkena sinar matahari maka pada sambungan itu akan mengalir arus listrik. Karakteristik kurva pada panel surya dapat dilihat pada gambar 2.2

Untuk struktur dari panel surya dapat dilihat pada Gambar 2.1



Gambar 2.1 Stuktur Panel Surya

(Sumber : teknologisurya.wordpress.com)



Gambar 2.2 Karakterisik Solar sel

Dari karakteristik solar sel pada gambar 2.2, maka daerah operasi sel surya berada di daerah MN pada kurva ketika nilai hambatan R kecil, dimana sel dianggap sebuah sumber arus konstan yang mendekati *short circuit current*. Jika R besar maka sel surya beroperasi di daerah PS pada kurva, dimana sel dianggap sebagai sumber tegangan konstan.

Besarnya energi listrik itu tergantung pada jumlah energi cahaya yang mencapai silikon itu dan luas permukaan sel itu (wikipedia.org 2010). Persamaan umum keluaran arus listrik pada panel surya adalah sebagai berikut [4]:

$$I = I_{pv} - I_o \left\{ exp\left[\frac{V + IR_s}{aV_t}\right] - 1 \right\} - \frac{V + IR_s}{R_p} \quad (2.1)$$

$$V_t = \frac{N_s kT}{q} \quad (2.2)$$

Keterangan :

I_{pv} adalah arus fotovoltaik (A),

I_o adalah arus saturasi dari dioda (A),

q adalah muatan elektron (1,602×10-19 C),

I adalah arus pada terminal fotovoltaik (A),

V adalah tegangan pada terminal fotovoltaik (V),

V_t adalah tegangan termal array,

k adalah konstanta Boltzman (1,381×10-23 J/K),

T adalah suhu sambungan p-n dalam Kelvin (K),

a adalah faktor idealitas dari dioda,

Rs adalah resistansi seri ekuivalen array fotovoltaik (Ohm),

Rp adalah resistansi paralel ekuivalen array fotovoltaik (Ohm),

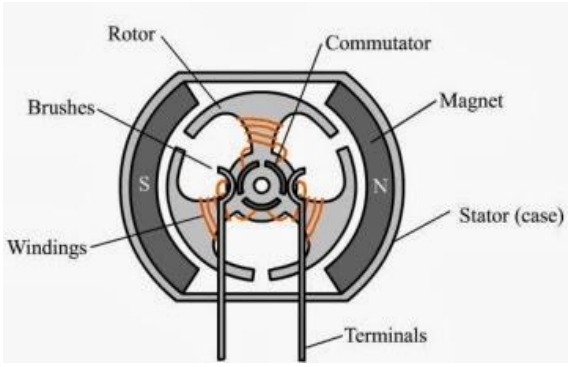
Ns adalah jumlah sel fotovoltaik terhubung seri.

2.3 Motor DC

Motor listrik merupakan perangkat elektromagnetis yang mengubah energi listrik menjadi energi mekanik. Fungsi energi mekanik ini digunakan untuk memutar *impeller* pompa, *fan* atau *blower*, menggerakan kompresor dan mengangkat bahan.

Sedangkan motor DC adalah sebuah motor listrik yang memerlukan suplai tegangan searah pada kumparan jangkar dan kumparan medan untuk diubah menjadi energi mekanik. Pada motor DC kumparan medan disebut stator (bagian yang tidak berputar) dan kumparan jangkar disebut rotor (bagian yang berputar). Bagian pada motor DC dapat dilihat pada gambar 2.3

Kebanyakan motor listrik beroperasi melalui interaksi medan magnet dan konduktor pembawa arus untuk menghasilkan kekuatan, meskipun motor elektrostatik menggunakan gaya elektrostatik. Proses sebaliknya, menghasilkan energi listrik dari energi mekanik, yang dilakukan oleh generator seperti alternator, atau dinamo. Banyak jenis motor listrik dapat dijalankan sebagai generator, dan sebaliknya. Motor listrik dan generator yang sering disebut sebagai mesin listrik.



Gambar 2.3. Bagian motor DC

(Sumber : www.webstudi.site/2019/08/Motor-DC)

Motor listrik DC (arus searah) merupakan salah satu dari motor DC. Mesin arus searah dapat berupa generator DC atau motor DC. Generator DC alat yang mengubah energi mekanik menjadi energi listrik DC. Motor DC alat yang mengubah energi listrik DC menjadi energi mekanik putaran. Sebuah motor DC dapat difungsikan sebagai generator atau sebaliknya generator DC dapat difungsikan sebagai motor DC.

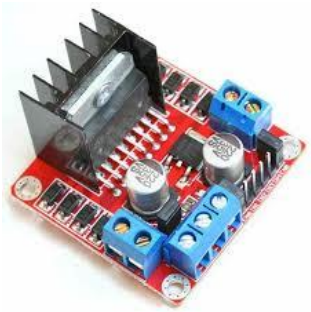
Pada motor DC kumparan medan disebut stator (bagian yang tidak berputar) dan kumparan jangkar disebut rotor (bagian yang berputar). Jika tejadi putaran pada kumparan jangkar dalam pada medan magnet, maka akan timbul tagangan (GGL) yang berubah-ubah arah pada setiap setengah putaran.

Prinsip dari arus searah adalah membalik phasa negatif dari gelombang sinusoidal menjadi gelombang yang mempunyai nilai positif dengan menggunakan komutator, dengan demikian arus yang berbalik arah dengan kumparan jangkar yang berputar dalam medan magnet.

2.4 Modul Driver L298

Modul driver L298 L298 adalah jenis IC driver motor yang dapat mengendalikan arah putaran dan kecepatan motor DC ataupun Motor stepper. Mampu mengeluarkan output tegangan untuk Motor dc dan motor stepper sebesar 50 volt dengan arus 4 Ampere. IC l298 terdiri dari transistor-transistor logik (TTL) dengan gerbang nand yang memudahkan dalam menentukkan arah putaran suatu motor dc dan motor stepper.

Modul driver ini berbasis H-Bridge. Dalam chip terdapat dua rangkaian H-Bridge. Selain itu driver ini mampu mengendalikan 2 motor sekaligus dengan arus beban 2 A. Rangkaian modul driver motor L298 dapat dilihat pada gambar 2.4.



Gambar 2.4. Modul driver L 298

Rangkaian modul driver motor yang terlihat pada gambar 2.4, menggunakan dioda sebagai output motor, hal ini bertujuan agar driver motor dapat menahan arus balik yang datang dari motor DC. Input driver motor berasal dari mikrokontroler utama, untuk MOT 1A dan MOT 1B untuk menggerakan motor 1, ENABLE 1 untuk mengatur kecepatan motor 1 menggunakan PWM, selanjutnya untuk MOT 2A dan MOT 2B untuk menggerakan motor 2, ENABLE 2 untuk mengatur kecepatan motor 2 menggunakan PWM.

2.5 Mikrokontroler Arduino Uno

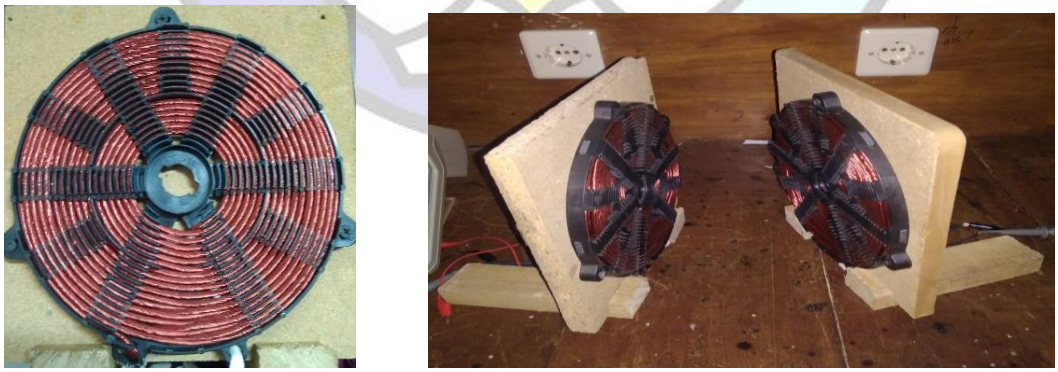
Arduino Uno adalah salah satu development kit mikrokontroler yang berbasis pada ATmega28. Arduino Uno merupakan salah satu board dari family Arduino. Modul ini sudah dilengkapi dengan berbagai hal yang dibutuhkan untuk mendukung mikrokontroler untuk bekerja, tinggal colokkan ke power suply atau sambungkan melalui kabel USB ke PC, Arduino Uno ini sudah siap bekerja. Arduino Uno board memilki 14 pin digital input/output, 6 analog input, sebuah resonator keramik 16MHz, koneksi USB, colokan power input, ICSP header, dan sebuah tombol reset. Arduino kuno sendiri merupakan sebuah mikrokontroler kita dapat membuat program untuk mengendalikan berbagai komponen elektronika. Fungsi Arduino Uno ini dibuat untuk memudahkan kita dalam melakukan prototyping, memprogram mikrokontroler, membuat alat-alat canggih berbasis mikrokontroler. Mikrokontroler arduino uno dapat dilihat pada gambar 2.4.

Gambar 2.5. Mikrokontroler Arduino Uno

(Sumber : /www.arduino.cc/en/Main/ArduinoBoardUnoSMD)

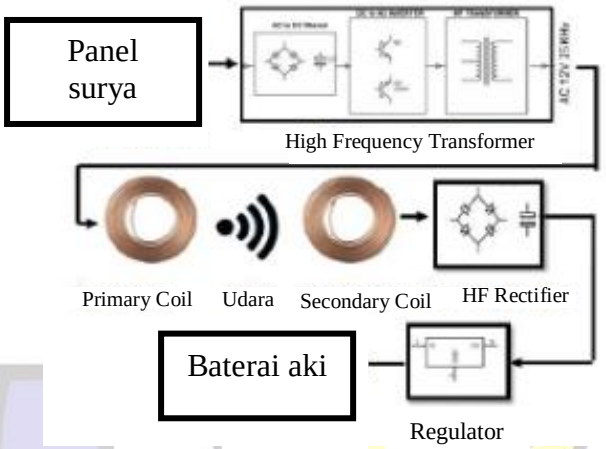
2.6 Sistem Transfer Daya Nirkabel

Sistem transfer daya nirkabel merupakan salah satu alternatif penyaluran daya listrik tanpa hubungan fisik berupa kabel. Pengiriman daya listrik tanpa kabel adalah suatu sistem yang memiliki proses dimana daya listrik dapat ditransmisikan dari suatu sumber listrik menuju beban tanpa melalui suatu kabel. Bagian utama sistem transfer daya ini adalah kumparan yang terdiri dari lilitan tembaga yang mempunyai diameter kawat 0,5 mm dengan diameter kumparan sebesar 19 cm.



Gambar 2.6. Kumparan primer dan sekunder

Sistem transfer daya nirkabel mempunyai 2 buah kumparan, yaitu kumparan primer dan kumparan sekunder. Energi listrik akan dialirkan dari kumparan primer kemudian akan diterima oleh kumparan sekunder. Energi yang dihasilkan oleh kumparan primer dalam bentuk garis gaya magnet (fluks) akan ditangkap oleh kumparan sekunder yang kemudian akan diubah menjadi tegangan DC untuk digunakan sebagai pengisian baterai. Blok diagram sistem pengisian nirkabel dapat dilihat pada gambar 2.7.



Gambar 2.7 Diagram Blok Sistem Transfer Daya Nirkabel

Tantangan utama yang dihadapi dalam transfer daya nirkabel adalah hilangnya garis-garis gaya magnet (fluks) dari sinyal yang ditransmisikan dengan jarak. Semakin panjang jarak antara kumparan primer dengan kumparan sekunder maka semakin kecil nilai efisiensi daya yang diterima, begitu juga sebaliknya. Sehingga untuk mendapatkan nilai efisiensi yang tinggi, jarak antar kumparan diperkecil dan meningkatkan nilai impedansi pada kumparan.

2.7 Sensor Suhu DS18B20

Sensor suhu DS18B20 adalah sensor suhu yang menggunakan interface one wire, sehingga hanya menggunakan kabel yang sedikit dalam instalasi nya. Unik nya sensor ini bisa di jadikan paralel dengan satu input. Artinya kita bisa menggunakan sensor DS18B20 lebih dari satu namun output sensor nya hanya di hubungkan ke satu PIN Arduino. Alasan ini membuat sensor ini banyak di gunakan, apalagi sensor ini memiliki tipe waterprof. Sensor suhu ini merupakan sensor digital yang memiliki 12-bit ADC internal. Sangat presisi, sebab jika tegangan referensi

sebesar 5Volt, maka akibat perubahan suhu, ia dapat merasakan perubahan terkecil sebesar $5/(2^{12}-1) = 0.0012$ Volt ! Pada rentang suhu -10 sampai +85 derajat Celcius, sensor ini memiliki akurasi +/-0.5 derajat. Sensor ini bekerja menggunakan protokol komunikasi 1-wire (one-wire). Gambar sensor DS28B20 dapat dilihat pada gambar 2.8.

Gambar 2.8 Gambar sensor suhu DS18B20

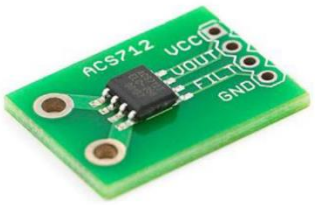
(Sumber : www.tutorialiot.com)

Sensor DS18B20 memiliki tiga kaki, yaitu GND (ground, pin 1), DQ (Data, pin 2), VDD (power, pin 3). Pada Arduino, VDD dikenal sebagai VCC. Dalam hal ini, kita asumsikan VCC sama dengan VDD. Tergantung mode konfigurasi, ketiga kaki IC ini harus dikonfigurasi terlebih dahulu. Sensor dapat bekerja dalam dua mode, yaitu mode normal power dan mode parasite power**.**

2.8 Sensor Arus ACS 712

ACS712 adalah *Hall Effect current* sensor. *Hall effect* allegro ACS712 merupakan sensor yang presisi sebagai sensor arus AC atau DC dalam pembacaan arus didalam dunia industri, otomotif, komersil dan sistem-sistem komunikasi. Pada umumnya aplikasi sensor ini biasanya digunakan untuk mengontrol motor, deteksi beban listrik, *switched-mode power supplies* dan proteksi beban berlebih, bentuk fisik dari sensor arus ACS712 dapat dilihat pada gambar 2.9.

Sensor ACS712 ini memiliki kekurangan yakni nilai arus yang di dapatkan dari sensor tidak linear sehingga terkadang kita membutuhkan tingkat linear yang lebih tinggi. ACS712 ini memiliki tipe variasi sesuai dengan arus maksimal yakni 5A, 20A, 30A. ACS712 ini menggunakan VCC 5V.

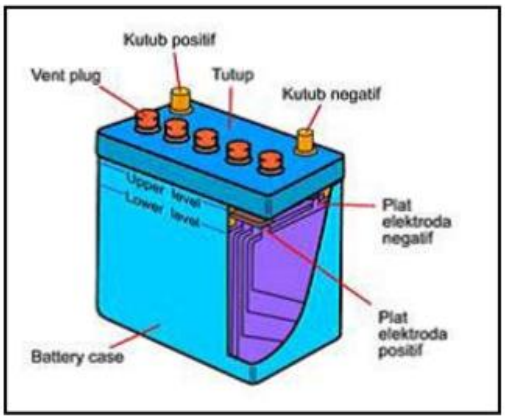


Gambar 2.9 Gambar sensor arus ACS712

(Sumber : http://ilmubawang.blogspot.com/2011/04/sensor-arus)

2.9 Karakteristik Aki

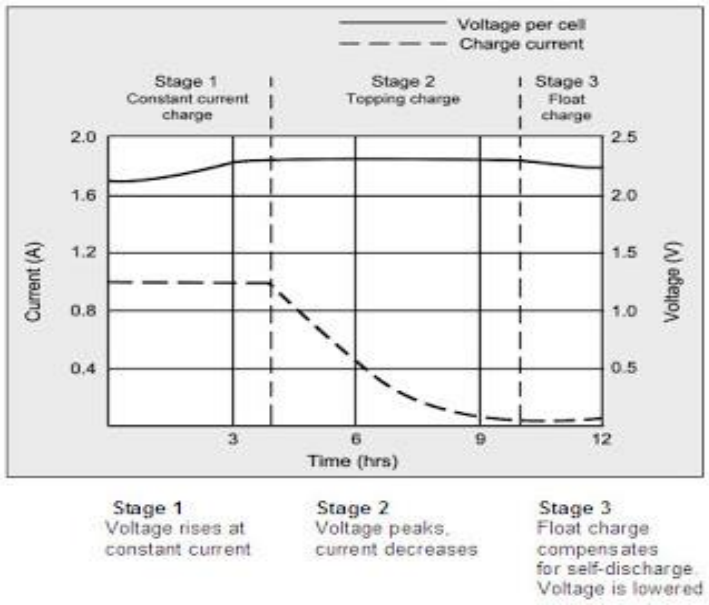
Aki merupakan media yang digunakan sebagai penyimpan arus listrik. Dalam aki ini terdapat jenis elemen dan sel untuk menyimpan arus yang mengandung asam sulfat (H_2SO_4). Tiap sel berisikan pelat positif dan negatif. Pada pelat positif terkandung oksidal timbal coklat (PbO_2), sedangkan pelat negatif mengandung timbal (Pb). Pelat-pelat ditempatkan pada batang penghubung. Pemisah atau separator menjadi isolasi diantara pelat itu, dibuat agar baterai acid mudah beredar disekeliling pelat. Bila ketiga unsur kimia ini berinteraksi, maka akan muncul arus listrik.



Gambar 2.10. Skema sel aki

(Sumber : /esdikimia.wordpress.com/2011/09/28/sel-volta)

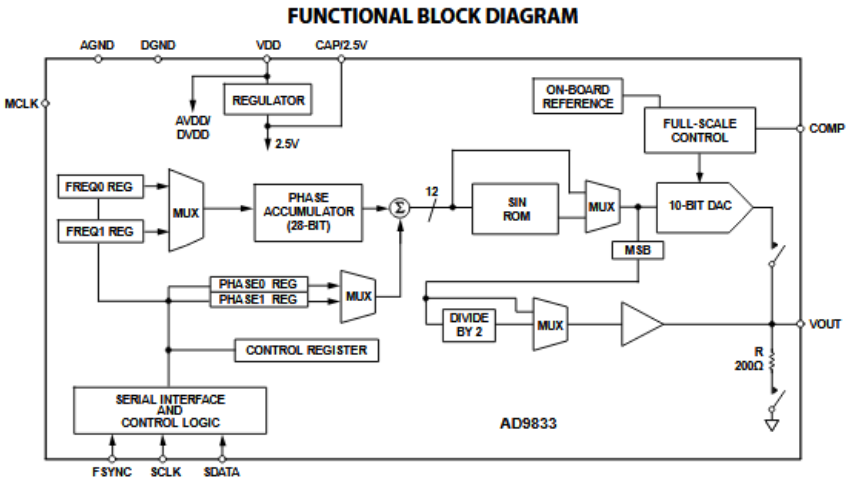
Baterai aki, terdiri dari beberapa sel. Baterai aki 12 Volt, terdiri dari 6 sel. Batas tegangan satu sel umumnya mulai dari 2.30V sampai 2.45V. Jadi baterai aki 12 Volt, tegangan sebenarnya adalah antara 13.8 V - 14.7 Volt. Kondisi baterai aki tergantung dari suhu. Suhu tinggi menyebabkan baterai cepat rusak. Pada saat pengisian baterai suhu pada elektrolit harus kurang dari 30˚C. Kurva pengisian aki dapat dilihat pada gambar 2.11.



Gambar 2.11. Kurva karakteristik pengisian aki

2.10 Programmable Waveform Generator AD9833

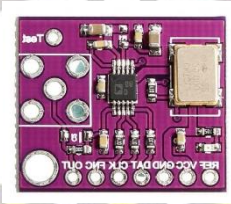
Modul AD9833 merupakan sebuah pembangkit sinyal gelombang daya rendah yang dapat diprogram dan mampu menghasilkan output gelombang sinus, segitiga, dan persegi. Pembentukan gelombang diperlukan dalam berbagai jenis aplikasi penginderaan, aktuasi, dan waktu domain reflectometry (TDR).



Gambar 2.12. Blok Diagram Waveform Generator

(Sumber : /www.researchgate.net/figure/Function-block-diagram-of-AD9833)

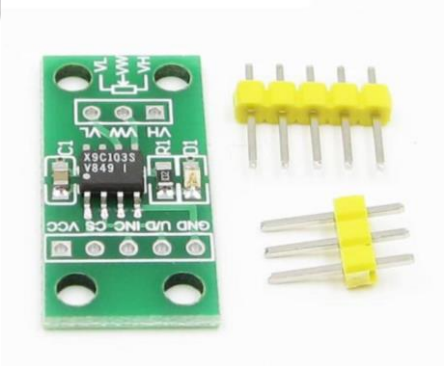
AD9833 dapat disetting ke resolusi 0,004 Hz. Frekuensi dan fase outputnya dapat diprogram sehingga dapat di set dengan mudah serta tidak diperlukan komponen eksternal. Registernya dapat mencapai lebar frekuensi 28 bit dengan clock rate 25 MHz, resolusi 0,1 Hz dan clock rate 1 MHz. AD9833 diprogram melalui komunikasi serial. Komunikasi serial ini beroperasi pada kecepatan hingga 40 MHz dan kompatibel dengan standar DSP dan mikrokontroler. Perangkat beroperasi dengan tegangan dari 2,3 V hingga 5,5 V. AD9833 memiliki fungsi mematikan (SLEEP). Fungsi ini memungkinkan bagian perangkat yang tidak digunakan akan dimatikan, sehingga meminimalkan konsumsi bagian saat ini. Misalnya, DAC dapat dimatikan saat output clock dihasilkan. AD9833 tersedia dalam paket MSOP 10-lead.



Gambar 2.13. Modul Programmable Waveform Generator

2.11 Modul X9C103

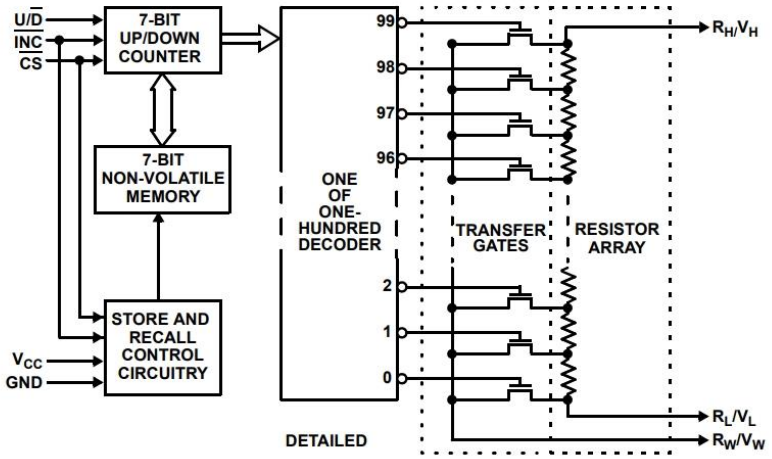
Modul X9C103 merupakan potensiometer digital 10 kΩ yang nilai resistansinya dapat diubah dengan memberikan input digital pada pin CS, U/D, dan INC menggunakan mikrokontroler arduino uno. Tampilan potensiometer digital X9C103 dapat dilihat pada gambar 2.14 dibawah ini



Gambar 2.14. Modul X9C103

(Sumber : ardushop.ro/en/home/991-x9c103s-digital-potentiometer-module)

Potensiometer digital ini memiliki 100 langkah penambahan dan pengurangan nilai resistansi, jadi jika terhubung di 5V, resolusi langkah keluaran penghapus akan sekitar 5V / 100 langkah = 50mV. Dua ujung potensiometer dapat dihubungkan ke tegangan yang menjangkau rentang hingga -5V hingga + 5V.Kemampuan sumber / sumber arus keluaran maksimum adalah 4.4mA. Blok diagram potensiometer digital ini dapat dilihat pada gambar 2.15



Gambar 2.15. Blok diagram X9C103

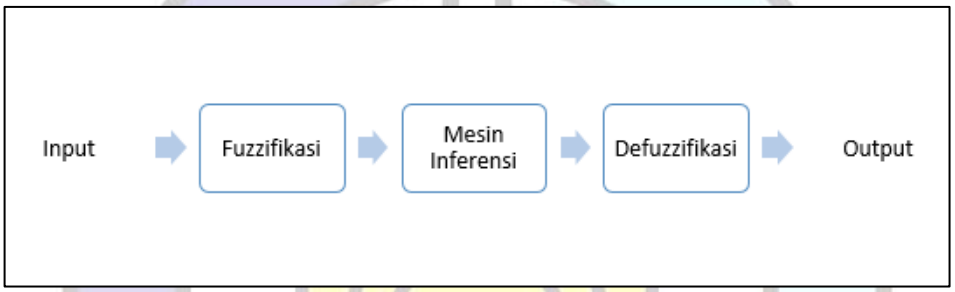
(Sumber : datasheetspdf.com/pdf/1327800/Renesas/X9C103)

2.12 Logika Fuzzy

Konsep logika *fuzzy* diperkenalkan oleh Prof. Lotfi Astor Zadeh pada tahun 1962. Logika *fuzzy* adalah metodologi sistem kontrol pemecahan masalah, yang cocok untuk diimplementasikan pada sistem yang sederhana, sistem kecil, embedded system, jaringan PC, multi-channel atau workstation berbasis akuisisi data, dan sistem kontrol. Metodologi ini dapat diterapkan pada perangkat keras, perangkat lunak, atau kombinasi keduanya. Dalam logika boolean dinyatakan bahwa segala sesuatu bersifat biner, yang artinya adalah hanya mempunyai dua kemungkinan, “Ya atau Tidak”, “Benar atau Salah”, dsb. Nilai keanggotaan dari logika boolean hanya 0 atau 1. Sedangkan dalam logika *fuzzy* memungkinkan nilai keanggotaan berada di antara 0 dan 1. Artinya, bisa saja suatu keadaan mempunyai

dua nilai “Ya dan Tidak”, “Benar dan Salah” secara bersamaan, namun besar nilainya tergantung pada bobot keanggotaan yang dimilikinya (Sutojo, et al., 2011).

Jika dibandingkan dengan logika konvensional, kelebihan logika *fuzzy* adalah kemampuannya dalam memproses penalaran secara bahasa sehingga dalam perancangannya tidak memerlukan persamaan matematik yang rumit. Beberapa alasan yang dapat diutarakan mengapa kita menggunakan logika *fuzzy* di antaranya adalah mudah dimengerti, memiliki toleransi terhadap data – data yang tidak tepat, dan mampu memodelkan fungsi-fungsi nonlinear yang sangat kompleks. Pemahaman tentang struktur dasar logika *fuzzy* diperlukan untuk mengerti tentang proses atau cara kerja dari logika *fuzzy*. Struktur dasar dari logika *fuzzy* dapat dilihat pada gambar 2.14.



Gambar 2.16. Struktur Dasar Logika *Fuzzy*

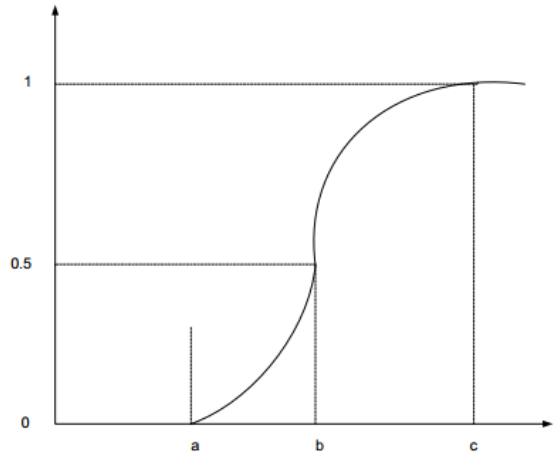
Penjelasan dari masing – masing gambar tersebut adalah sebagai berikut:

a. Input merupakan data masukkan yang berupa nilai tegas (crisp).
b. Fuzzifikasi yaitu proses untuk mengubah data input menjadi himpunan fuzzy dalam bentuk variabel linguistik. Penentuan keanggotaan suatu himpunan fuzzy tidak dibatasi oleh aturan – aturan tertentu. Ada beberapa macam fungsi keanggotaan yang dinyatakan dalam fungsi keanggotaan S (Sigmoid), π (Pi), dan T (Triangular).
    1. Fungsi keanggotaan Sigmoid.

       Fungsi keanggotaan Sigmoid dapat dilihat pada persamaan (2.3).

$$S(x:a,b,c) = \begin{cases} 0 & \rightarrow \quad x \leq a \\ 2((x-a)/(c-a))^2 & \rightarrow a \leq x \leq b \\ 1-2((c-x)/(c-a))^2 & \rightarrow b \leq x \leq c \\ 1 & \rightarrow \quad x \geq c \end{cases} \quad (2.3)$$

Bentuk diagram fungsi keanggotaan Sigmoid dapat dilihat pada gambar 2.15.



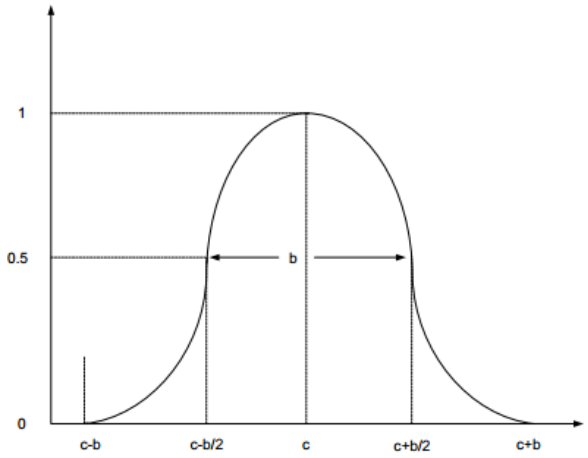
Gambar 2.17. Grafik Fungsi Keanggotaan Sigmoid

2. Fungsi keanggotaan Pi.

   Fungsi keanggotaan Pi dapat dilihat pada persamaan (2.4).

$$\pi(x: b, c) = \begin{cases} S\big(x; (c-b), \big(c-(b/2)\big), c\big) & \rightarrow x \leq c \\ 1 - S\Big(x; c, \big(c+(b/2)\big), (c+b)\Big) & \rightarrow x > c \end{cases} \quad (2.4)$$

   Bentuk diagram fungsi keanggotaan Pi dapat dilihat pada gambar 2.16.



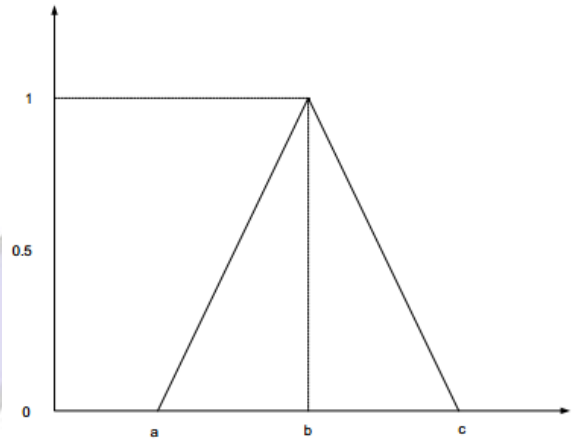
Gambar 2.17 Fungsi Keanggotaan Pi

3. Fungsi keanggotaan Triangular.

   Fungsi keanggotaan Triangular dapat dilihat pada persamaan (2.5).

$$T(x: a, b, c) = \begin{cases} 0 & \rightarrow \quad x \leq a \\ (x-a)/(b-a) & \rightarrow a \leq x \leq b \\ (c-x)/(c-b) & \rightarrow b \leq x \leq c \\ 0 & \rightarrow \quad x \geq c \end{cases} \qquad (2.5)$$

Bentuk diagram fungsi keanggotaan Triangular dapat dilihat pada gambar 2.17.



Gambar 2.18. Grafik Fungsi Keanggotaan Triangular

c. Mesin inferensi merupakan proses untuk mengubah input fuzzy menjadi output fuzzy dengan cara mengikuti aturan – aturan (Rules) yang telah ditetapkan. Kumpulan aturan (Rules) fuzzy berupa pernyataan IF ... THEN. Mesin inferensi dapat dilakukan dengan menggunakan beberapa fungsi sebagai berikut:
   1. Fungsi implikasi min digunakan untuk mendapatkan nilai α – predikat hasil implikasi dengan cara memotong output himpunan fuzzy sesuai dengan derajat keanggotaan yang terkecil.
   2. Fungsi implikasi dot digunakan untuk mendapatkan nilai α – predikat hasil implikasi dengan cara menskala output himpunan fuzzy sesuai dengan derajat keanggotaan yang terkecil.

d. Defuzzifikasi merupakan proses pengubahan besaran fuzzy (variabel linguistik) yang disajikan dalam bentuk himpunan – himpunan output fuzzy dengan fungsi keanggotaannya untuk mendapat kembali bentuk tegasnya

(crisp). Defuzzifikasi dapat dilakukan dengan menggunakan metode sebagai berikut:

1. *Maximum of Mean*.

   Metode *Maximum of Mean* didefinisikan pada persamaan (2.6).

$$V_o = \sum_{i=1}^{j} \frac{v_i}{J} \tag{2.6}$$

   Di mana V_o merupakan nilai keluaran, J merupakan jumlah harga maksimum, dan V_i merupakan nilai keluaran maksimum ke-j.

2. *Center of Area*

   Metode *Center of Area* sering disebut juga sebagai metode *Center of Gravity* yang didefinisikan pada persamaan (2.7).

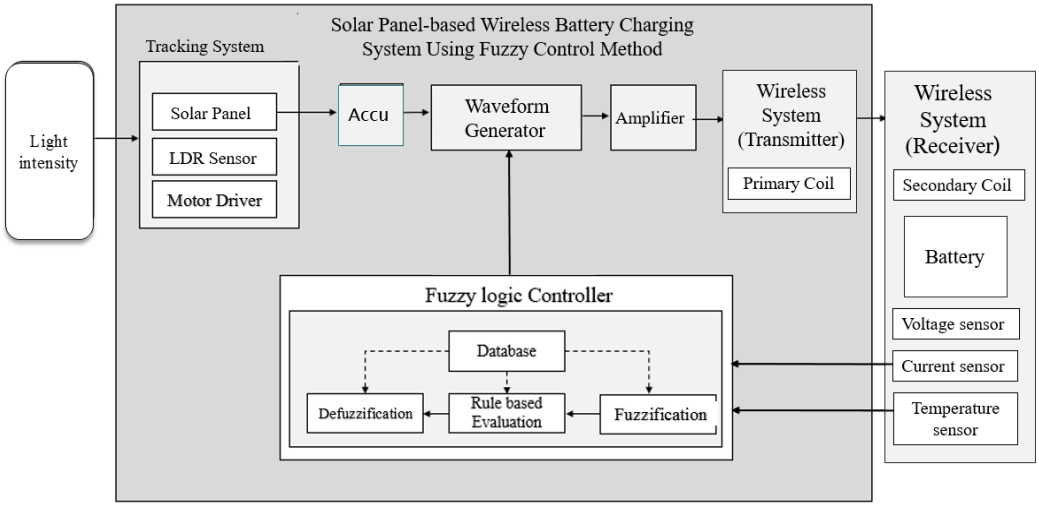
$$V_o = \frac{\sum_{k=1}^{m} V_k \mu_v(V_k)}{\sum_{k=1}^{m} \mu_v(V_k)} \tag{2.7}$$

   Di mana V_o merupakan nilai keluaran, m merupakan tingkat kuantisasi, V_k merupakan elemen ke-k, $\mu_v(V_k)$ merupakan derajat keanggotaan elemen-elemen pada *fuzzy set V*, dan V merupakan semesta pembicaraan.

BAB 3
DESAIN DAN PEMBUATAN SISTEM

Pengujian dimaksudkan untuk mendapatkan evaluasi terhadap rangkaian, agar diperoleh kinerja yang lebih baik. Kinerja yang lebih baik didapatkan dengan melakukan perbaikan terhadap komposisi rangkaian yang mengalami kekeliruan yang diketahui saat melakukan pengujian. Pengujian beberapa sistem perlu dilakukan untuk mengetahuisistem dapat bekerja dengan baik dan dapat mengetahui karakteristik setiap sistem yang dibuat.

Sistem pengisian baterai secara wireless ini mempunyai beberapa pengujian yang akan dilakukan, seperti pengujian pada sistem tracking, pengujian pada sistem wireless, dan pengujian keseluruhan sistem dengan menggunakan metode fuzzy. Secara garis besar blok sistem akan ditunjukkan pada gambar 3.1. yang terlihat dibawah ini.

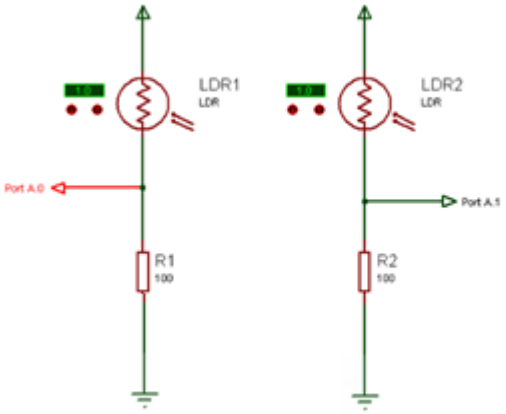


Gambar 3.1. Diagram keseluruhan blok sistem pengisian baterai nirkabel

3.1 Pengujian sistem tracking panel surya

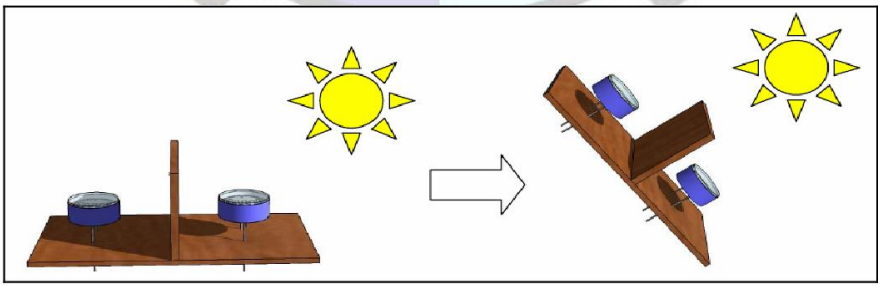
Pada pengujian kali ini panel surya menggunakan sensor LDR yang dirangkai seri dengan resistor 100 Ohm. Rangkaian ini berfungsi sebagai mengukur nilai tegangan yang berubah akibat nilai resistansi pada LDR yang berubah akibat

terkena intensitas cahaya matahari. Sensor LDR yang akan digunakan mempunyai skematik seperti pada gambar 3.2.



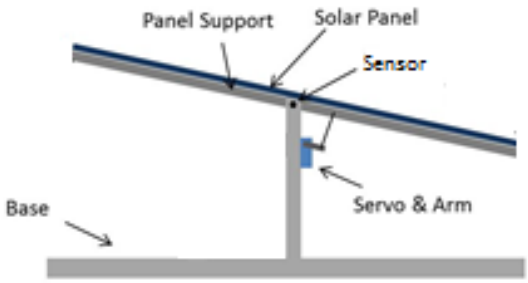
Gambar 3.2. Skematik rangkaian sensor LDR

Pembuatan sensor LDR ini dibuat dengan cara disusun sejajar kemudian ditengahnya diberi pembatas sebagai dinding untuk membuat bayangan ketika sensor tidak tegak lurus dengan arah datangnya sinar. Rancang sensor LDR ini bertujuan agar sensor dapat membedakan posisi matahari. Ketika matahari tidak berada tegak lurus sensor 1, maka akan timbul bayangan dari pembatas yang mengenai sensor 2, sehingga nilai tegangan sensor akan berbeda. Hal ini akan membuat mikrokontroler menggerakkan motor ke arah datangnya sinar matahari, hingga kedua buah sensor LDR sama-sama terkena sinar matahari. Prinsip kerja LDR pada tracking panel surya dapat dilihat pada gambar 3.3.



Gambar 3.3. Prinsip kerja LDR pada tracking panel surya

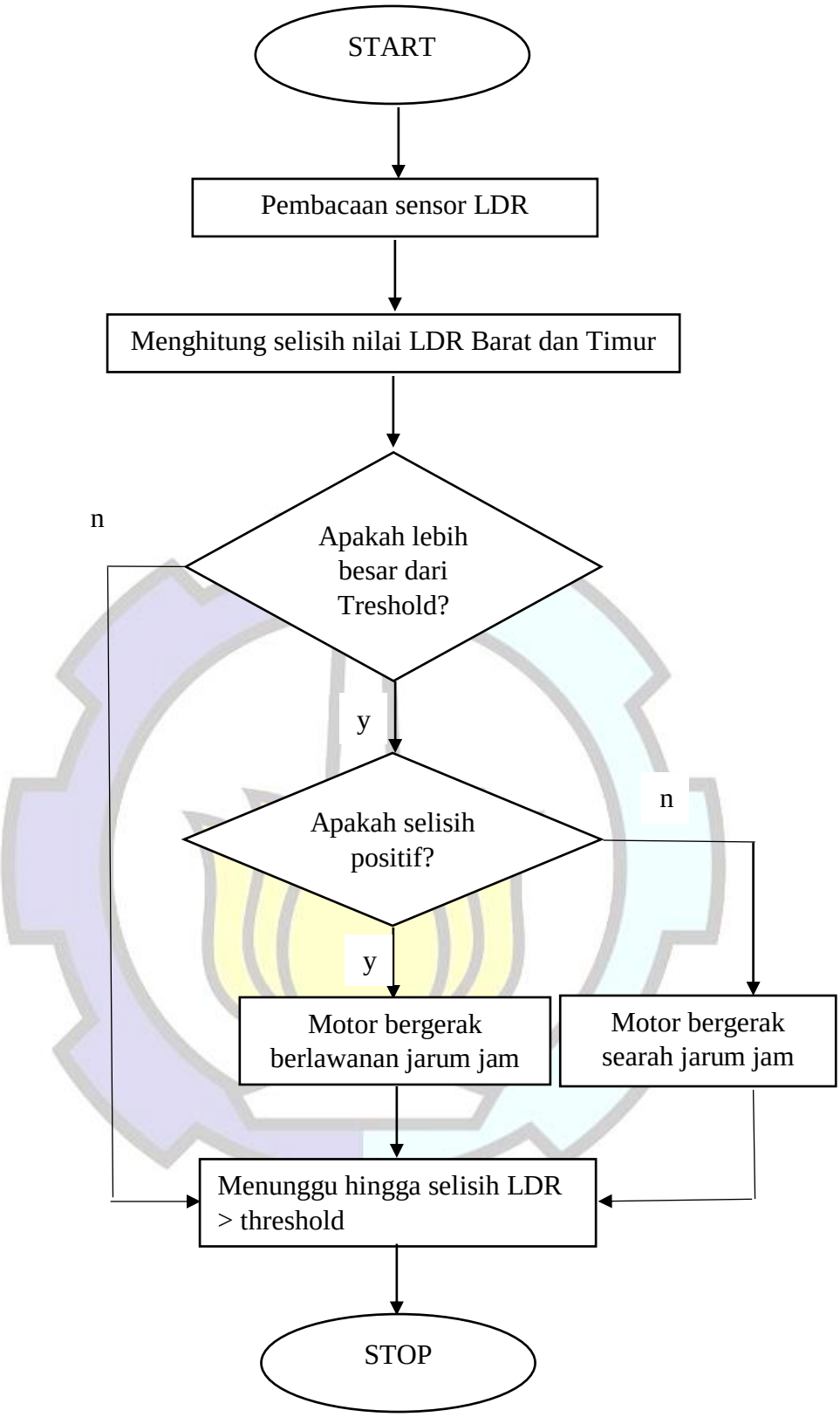
Pergerakkan sensor LDR pada tracking panel surya ini dikarenakan sensor menempel pada bagian rangka panel surya, sehingga pergerakkan rangka panel akan mengikuti arah datangnya sinar seperti prinsip kerja pada sensor LDR. Sistem tracking secara keseluruhan dapat dilihat pada gambar 3.4.



Gambar 3.4. Sistem tracking secara keseluruhan

Sistem tracking pada panel surya terdiri dari panel surya, rangka panel, motor DC dan sensor LDR. Sistem ini dapat mengikuti arah datangnya sinar matahari dari ufuk timur hingga ufuk barat dengan bantuan sensor LDR. Pergerakkan motor akan berhenti ketika jumlah intensitas yang diterima kedua sensor LDR hampir sama (memiliki tegangan yang hampir sama). Ketika malam hari dan tidak ada intensitas cahaya matahari yang masuk, motor akan berhenti bergerak hingga ada cahaya yang mengenai sensor LDR dan mengakibatkan perbedaan intensitas cahaya pada kedua buah sensor. Sistematika pergerakkan sistem tracking ini dapat dilihat pada flowchat di gambar 3.5.

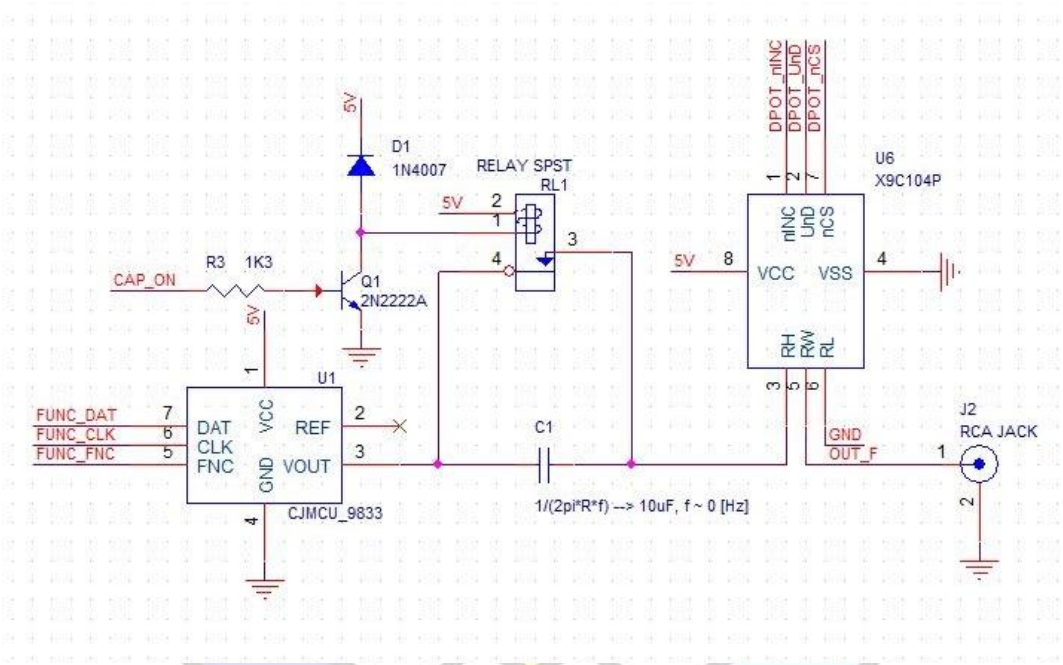
Pada flowchart sistem pergerakkan tracking panel surya, dapat dilihat bahwa sistem akan mendeteksi secara terus menerus terhadap intensitas cahaya yang mengenai 2 buah sensor LDR. Sistem mikrokontroler akan membandingkan selisih nilai dari 2 buah sensor LDR yang terkena intensitas cahaya. Ketika nilai tegangan sensor yang terbaca melebihi nilai treshold maka motor akan menggerakkan panel surya, negitu juga sebaliknya ketika selisih dari nilai 2 buah sensor LDR tersebut kurang dari nilai treshold maka motor akan berhenti bergerak. Hal ini di bertujuan agar motor tidak selalu bekerjasaat terjadi perbedaan intensitas yang sedikit, sehingga energi untuk motor dapat lebih hemat.



Gambar 3.5. Flowchart sistem tracking panel surya

3.2 Sistem kontrol waveform generator

Sistem kontrol waveform generator terdiri dari tiga modul yaitu waveform generator AD9833 yang berfungsi sebagai pembangkit bentuk sinyal dan pengatur frekuensi gelombang, yang kedua adalah modul X9C103 sebagai kontrol amplitudo sinyal yang akan dibangkitkan, serta modul yang ketiga adalah modul apmlifier TDA7386 yang berfungsi sebagai penguat output sinyal yang akan ditransmisikan ke kumparan primer sebagai sistem charging. Skematik sistem kontrol waveform generator ini dapat dilihat pada gambar 3.6.



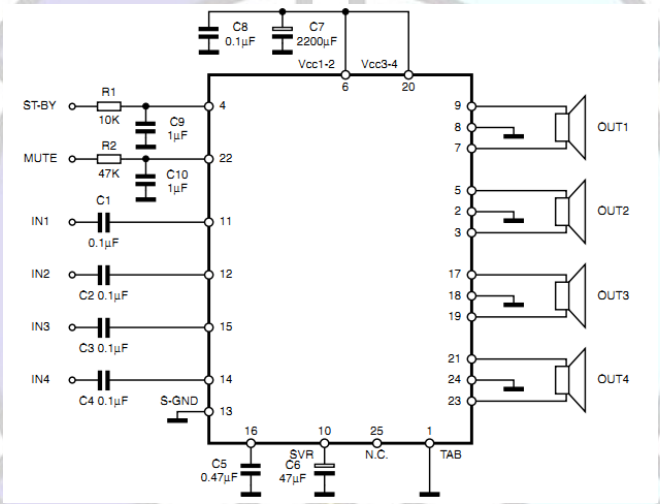
Gambar 3.6. Skematik sistem kontrol waveform generator

Modul waveform generator di kontrol oleh mikrokontroler arduino uno dengan 3 input, yaitu CLK, DAT, dan FNC. Dari kontrol ini berbagai bentuk sinyal dapat dibuat seperti sinyal sinus, sinyal kotak, dan sinyal segitiga. Modul waveform generator ini juga dapat mengatur nilai frekuensi yang akan dibangkitkan. Mulai dari 1 Hz hingga 10 MHz. Output dari sinyal waveform generator ini kemudian di masukkan ke dalam modul X9C103 sebagai input.

Modul X9C103 ini merupakan potensiometer digital yang nilainya diatur oleh 3 input digital, yaitu INC, U/D, dan CS. 3 input ini dihubungkan ke arduino uno untuk menghasilkan nilai tegangan sehingga nilai outputnya dapat dikontrol oleh arduino. Sinyal input yang berupa nilai sinus akan dimasukkan ke

potensiometer digital untuk diatur nilai amplitudonya, sehingga nilai amplitudo outputnya dapat di kontrol oleh sistem fuzzy pada pengujian secara keseluruhan nantinya.

Modul amplifier TDA7386 merupakan modul amplifier yang berfungsi sebagai penguat daya sinyal output yang berasal dari waveform generator dan potensiometer digital X9C103. Supply daya amplifier ini berasal dari aki yang berada sistem tracking panel surya yang diubah bentuk gelombangnya agar dapat ditransmisikan melalui kumparan primer, sehingga sistem pengisian daya nirkabel dapat terjadi. Gambar rangkaian amplifier TDA 7386 dapat dilihat pada gambar 3.7 dibawah ini.



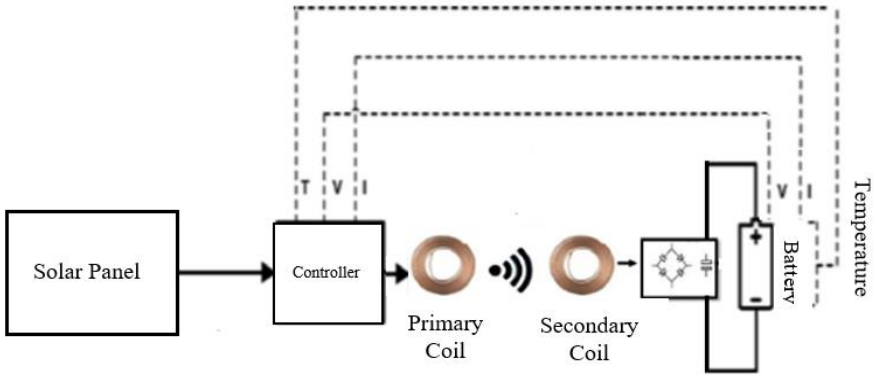
Gambar 3.7. Rangkaian amplifier TDA7386

Sinyal yang berbentuk sinus dengan frekuensi 90 kHz hasil output waveform generator akan dinaikkan daya nya untuk proses transfer daya nirkabel menuju kumparan primer dan akan ditangkap oleh kumparan sekunder, sehingga daya yang diterima kumparan sekunder lebih besar untuk kemudian dilakukan pengisian pada baterei.

3.3 Sistem Pengisian Daya Nirkabel

Sistem pengisian daya nirkabel terdiri dari beberapa komponen utama yaitu kumparan primer, kumparan sekunder, rectifier (penyearah), baterai, sensor arus,

dan sensor suhu. Diagram blok sistem transfer daya listrik nirkabel untuk mengisi baterai ditunjukkan pada gambar 3.8 dibawah ini.



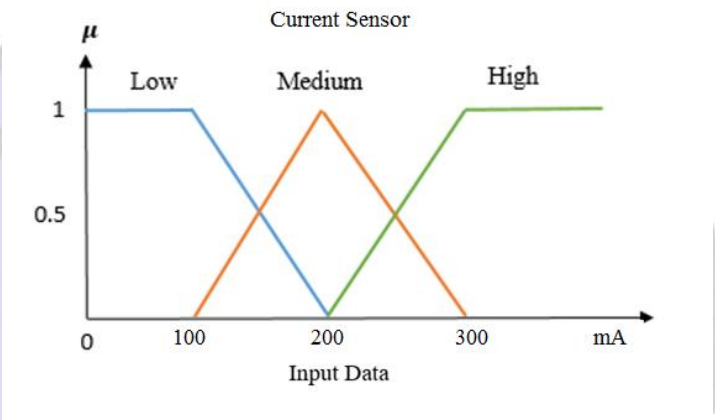
Gambar 3.8. Sistem pengisian nirkabel

Sistem pengisian daya nirkabel ini membutuhkan tegangan AC dengan frekuensi 90 kHz agar dapat menghasilkan nilai osilasi saat melewati kumparan primer. Pada kumparan primer akan menghasilkan nilai gaya gerak listrik (fluks) yang akan ditangkap oleh kumparan sekunder. Fluks yang ditangkap oleh kumparan sekunder kemudian dilewatkan ke rectifier (penyearah) untuk dijadikan tegangan DC yang akan digunakan sebagai sumber charging pada baterai. Selama terjadi pengisian daya secara nirkabel pada baterai terdapat sensor arus dan sensor suhu yang digunakan untuk monitoring keadaan baterai.

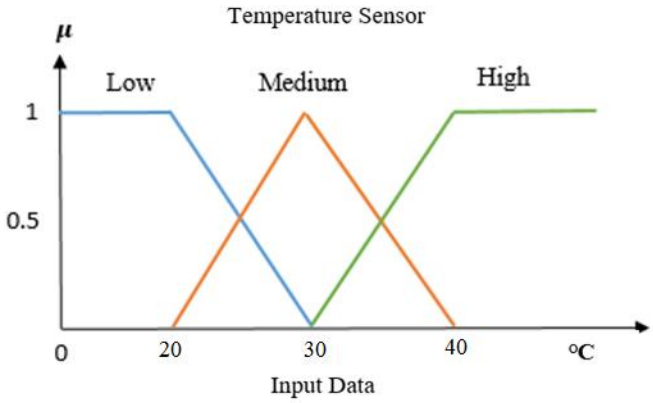
Sistem fuzzy digunakan pada saat terjadi pengisan daya nirkabel berlangsung. Sistem fuzzy akan mendeteksi tegangan baterai ketika baterai dalam keadaan kosong saat awal pengisian sehingga fuzzy akan memberikan perintah di dalam mikrokontroler untuk menaikkan tegangan input, sehingga tegangan input akan menjadi besar dan sistem pengisian daya akan berlangsung cepat dengan nilai arus yang besar. Selama pengisian berlangsung sensor arus dan sensor suhu akan monitoring nilai arus yang masuk pada baterai dan temperatur pada baterai. Jika terjadi terlalu lama pengisian pada baterai dan baterai mulai penuh, maka temperatur pada baterai akan naik, hal ini akan menyebabkan umur baterai menjadi lebih cepat sehingga untuk mencegah hal tersebut sistem fuzzy akan menurunkan tegangan input saat pengisian, sehingga arus yang masuk pada bahtera akan

berkurang. Sistem fuzzy akan memberikan perintah menurunkan tegangan input ketika suhu pada baterai naik dan arus yang masuk pada baterai terlalu besar, hal ini akan terus berlanjut hingga baterai penuh dan sistem fuzzy akan menghentikan pengisian pada baterai.

Batasan nilai arus yang dapat dialirkan ke dalam baterai saat pengisian serta batasan nilai suhu baterai yang terukur terdapat pada aturan input membership function fuzzy. Input membership function fuzzy arus dapat dilihat pada gambar 3.9 dibawah ini. Sedangkan untuk input membership function fuzzy temperatur dapat dilihat pada gambar 3.10.



Gambar 3.9. Input membership function arus



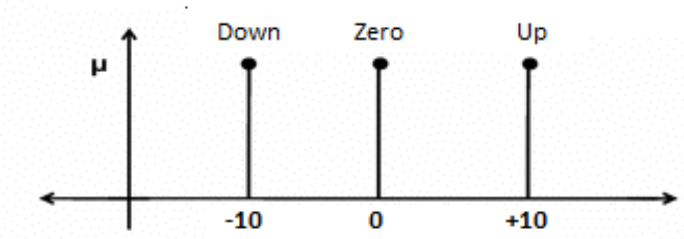
Gambar 3.10. Input membership function temperatur

Setiap nilai arus yang terukur pada sensor ACS712 dan nilai temperatur yang terukur pada sensor DS18B20 pada baterai akan dimasukkan ke dalam membership function fuzzy untuk menentukan keputusan yang akan diambil oleh logika fuzzy. Keputusan yang diambil logika fuzzy tergantung dari rute base yang diberikan pada fuzzy. Rule base logika fuzzy pada sistem dapat dilihat pada gambar 3.11 dibawah ini.

T \ I	I_L	I_M	I_H
T_L	Up	Up	Zero
T_M	Up	Zero	Down
T_H	Zero	Down	Down

Gambar 3.11 Rule base pada kontrol logika fuzzy

Setelah logika fuzzy menentukan keputusan dalam pengambilan keputusan sesuai rule base pada kontrol logika fuzzy, maka fuzzy akan mengeluarkan output sesuai output membership function sehingga nilai tegang input yang akan ditransmisikan ke kumparan sekunder dapat dikontrol. Output membership function pada ligika fuzzy dapat dilihat pada gambar 3.12 dibawah ini.



Gambar 3.12. Output membership function pada logika fuzzy

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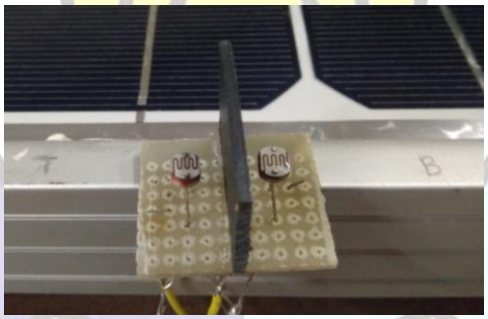
BAB 4
HASIL DAN PEMBAHASAN

Pengujian yang dilakukan pada penelitian ini meliputi, perancangan dan pengujian tracking panel surya, perancangan function generator, pengujian beberapa frekuensi osilasi untuk proses wireless charching, dan pengujian alat secara keseluruhan dengan menggunakan metode fuzzy. Kemudian hasil dari implementasi dianalis pada bab ini.

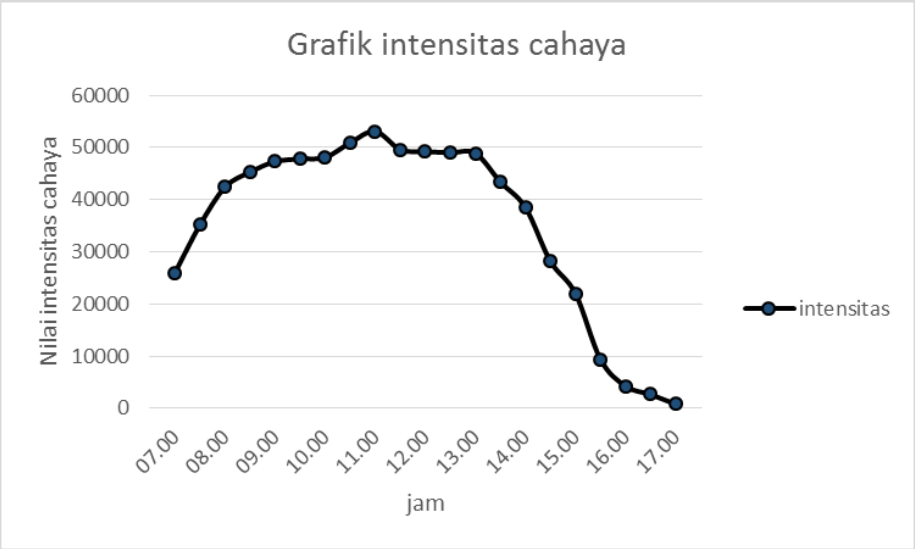
4.1 Perancangan Solar Tracking

Pada awal perancangan tracking panel surya ini dilakukan pengujian nilai sensor LDR yang akan menjadi sensor untuk pergerakkan tracking panel surya. Pesangan 2 buah LDR disusun sejajar kemudian diberikan pembatas ditengahnya. Hal ini bertujuan agar sensor LDR dapat memberikan nilai yang berbeda ketika sudut cahaya tidak tegak lurus terhadap panel surya. Bentuk rangkaian sensor LDR dapat dilihat pada gambar 4.1 dibawah ini.



Gambar 4.1. Rangkaian sensor LDR pada tracking panel surya

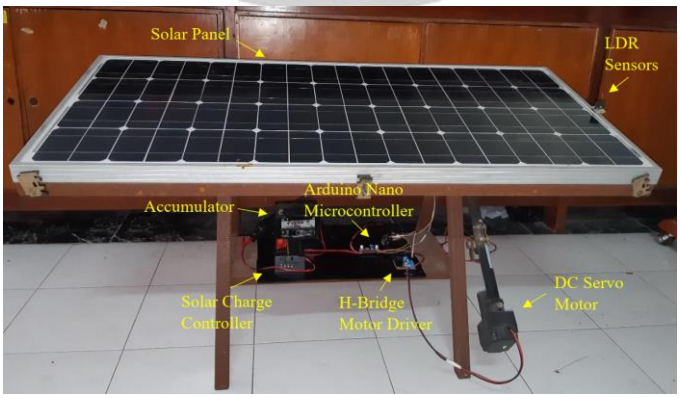
Ketika intensitas cahaya matahari mengenai sensor LDR, maka nilai tegangan akan berubah akibat nilai resistansi pada LDR berubah. Nilai ini kemudian dicatat untuk mengukur perubahan nilai tegangan tiap 30 menit. Perbandingan nilai tegangan pada resistansi sensor LDR dengan nilai intensitas cahaya yang terukur pada luks meter kemudian dicatat dan ditampilkan pada grafik yang terlihat pada gambar 4.2.



Gambar 4.2. Grafik intensitas cahaya yang diterima LDR

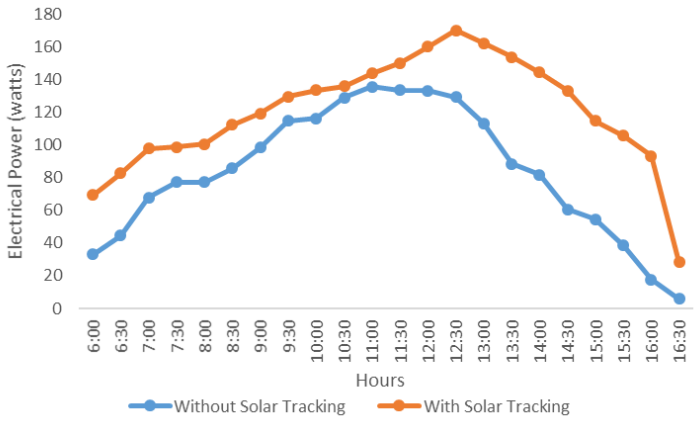
Pada gambar 4.2 terlihat bahwa nilai intensitas cahaya matahari yang terukur akan semakin tinggi hingga siang hari pada jam 11.30, kemudian intensitas cahaya matahari akan turun hingga sore hari pada jam 17.00. Pengukuran tegangan pada sensor LDR juga sebanding dengan nilai intensitas cahaya matahari yang ditangkap oleh sensor LDR, semakin besar nilai intensitas matahari maka semakin besar pula nilai tegangan sensor LDR yang dihasilkan.

Pada sistem tracking, panel surya yang dipergunakan adalah panel surya dengan daya 100 WP. Pengujian panel surya merupakan pengujian awal secara hardware, dimulai dari pengukuran tegangan keluaran panel surya pada pukul 07.00 hingga 17.00. Bentuk fisik sistem tracking panel surya yang telah dibuat dapat dilihat pada gambar 4.3 dibawah ini.



Gambar 4.3 Solar tracking

Pengukuran hasil output panel surya dengan menggunakan sistem pelacakan pada panel surya dicatat dan dibandingkan dengan pengukuran hasil output panel surya tanpa sistem tracking. Hasil perbandingan nilai output tersebut ditampilkan melalui grafik pada gambar 4.4 dibawah ini.

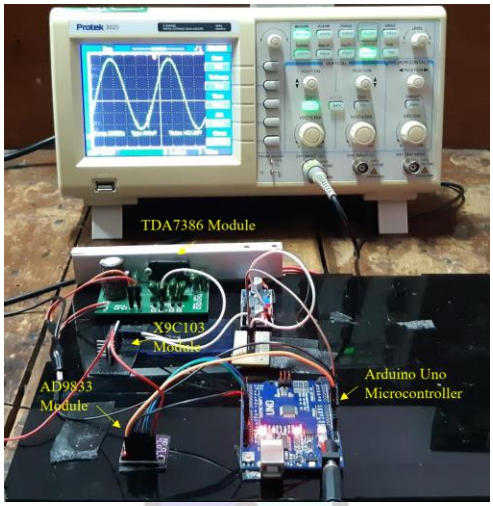


Gambar 4.4 Grafik daya output solar panel tanpa tracking dan dengan tracking

Dari gambar 4.4 diatas dapat kita lihat bahwa menggunakan sistem tracking pada panel surya dapat meningkatkan nilai intensitas cahaya yang ditangkap. Hal ini dikarenakan sistem tracking dapat mengikut arah datangnya sinar matahari, sehingga intensitas yang diterima lebih banyak, semakin banyak intensitas yang diterima panel surya, maka semakin besar pula daya yang dihasilkan. Perhitungan dari grafik padagambar 4.4 dapat disimpulkan bahwa penggunaan sistem tracking ini dapat menghasilkan energi listrik hingga 44% dibanding dengan tanpa tracking.

4.2 Waveform Generator

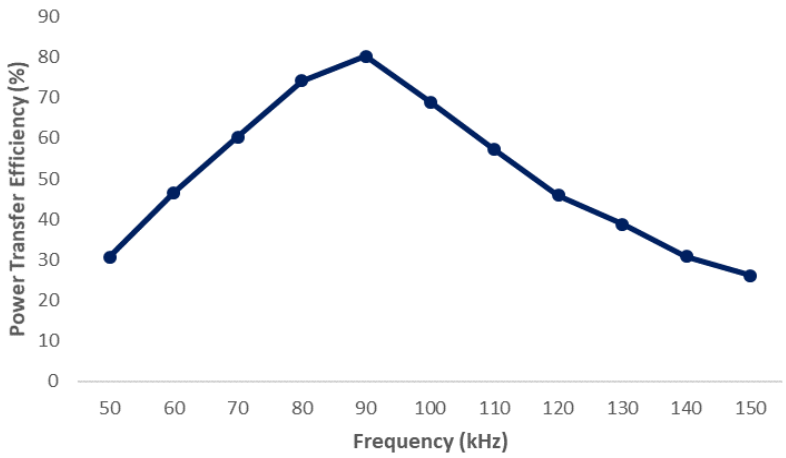
Perancangan waveform generator dilakukan untuk menghasilkan gelombang yang sesuai dengan frekuensi osilasi yang dibutuhkan pada sistem wireless charching sehingga didapatkan daya yang maksimal. Perancangan dan uji coba waveform generator ini dapat dilihat pada gambar 4.5.



Gambar 4.5 Pembuatan waveform generator dengan pada frekuensi 90 kHz

Pada perancangan waveform generator dihasilkan beberapa gelombang sinyal output, yaitu gelombang sinus, kotak dan segitiga. Gelombang sinus dapat menghasilkan bentuk gelombang output yang optimal daripada bentuk gelombang yang lain, dikarenakan nilai tegangan yang berubah terhadap waktu dibutuhkanuntuk perubahan nilai luks untuk proses osilasi pada kumparan primer dan kumparan sekunder.

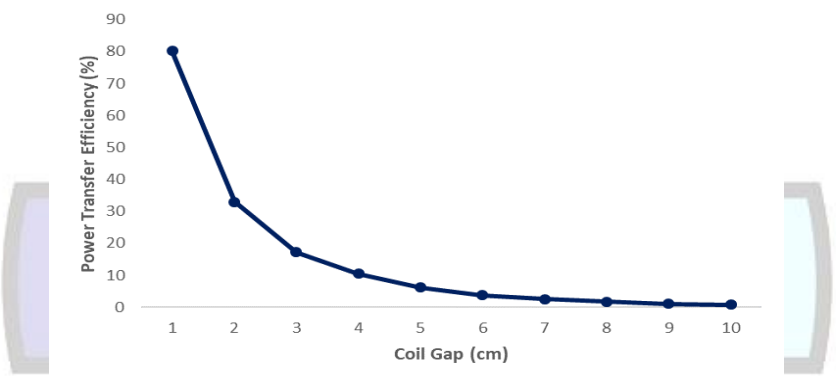
Pengujian beberapa kali dilakukan untuk mendapatkan nilai frekuensi gelombang yang maksimal. Uji coba dilakukan dari frekuensi 50 kHz hingga 150 kHz, lalu hasil output dicatat dan ditampilkan dalam grafik pada gambar 4.6 dibawah ini.



Gambar 4.6. Grafik efisiensi transfer daya terhadap frekuensi

Dari hasil pengamatan pada grafik efisiensi daya terhadap frekuensi yang ditransmisikan dapat disimpulkan bahwa nilai frekuensi osilasi maksimal yang digunakan sebesar 90 kHz. Nilai frekuensi osilasi ini digunakan untuk mentransmisikan daya dari kumparan primer menuju kumparan sekunder, sehingga daya yang dapat ditransmisikan lebih maksimal daripada menggunakan frekuensi yang lain.

Pengujian selanjutnya dilakukan untuk mengetahui efisiensi daya terhadap jarak antar kumparan. Pengukuran dan pencatatan nilai daya output dilakukan dengan jarak antar kumparan yaitu 1 cm hingga 10 cm. Kemudian hasil dari data output tersebut ditampilkan dengan grafik pada gambar 4.7 dibawah ini.



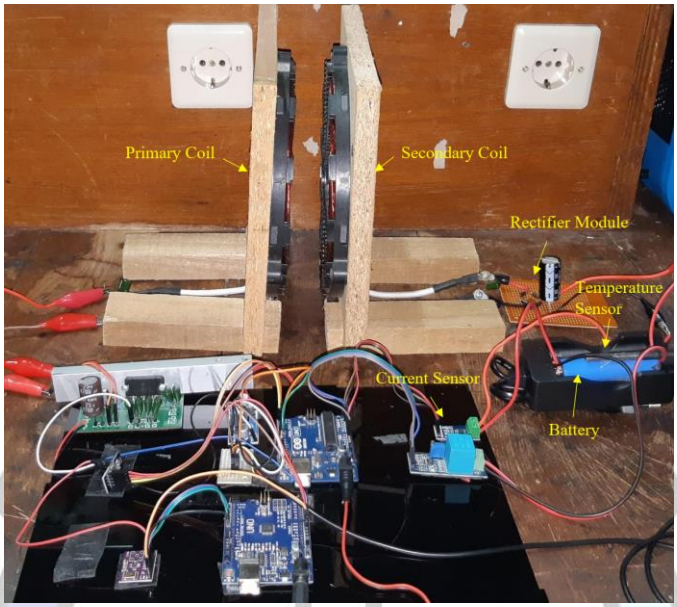
Gambar 4.7. Grafik efisiensi transfer daya terhadap jarak antar kumparan

Dari grafik efisiensi daya pada gambar 4.7 diatas dapat disimpulkan bahwa semakin panjang jarak antar kumparan, maka efisiensi daya akan semakin rendah begitu juga sebaliknya, semakin dekat jarak antar kumparan maka akan semakin besar nilai efisiensi daya yang dihasilkan. Sehingga pada sistem pengisian nirkabel ini jarak yang digunakan antar kumparan sebesar 1 cm agar mendapatkan efisiensi daya yang maksimal.

4.3 Pengujian secara keseluruhan

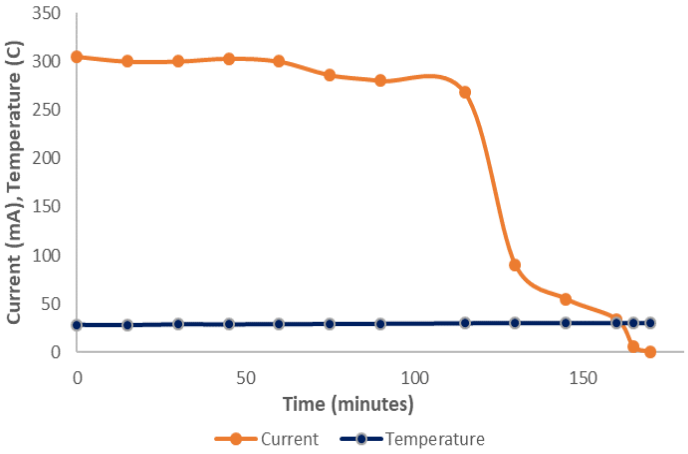
Pada pengujian kali ini merupakan pengujian secara keseluruhan terhadap sistem yang dibuat. Pengujian kali ini menggunakan metode fuzzy pada sistem pengisian baterai secara nirkabel. Pengujian sistem pengisian nirkabel ini dilakukan beberapa menit untuk mengetahui kondisi baterai dari keadaan kosong hingga

keadaan penuh. Baterai yang digunakan adalah baterai recharge 3,2 volt. Pengujian alat secara keseluruhan dapat dilihat pada gambar 4.8.



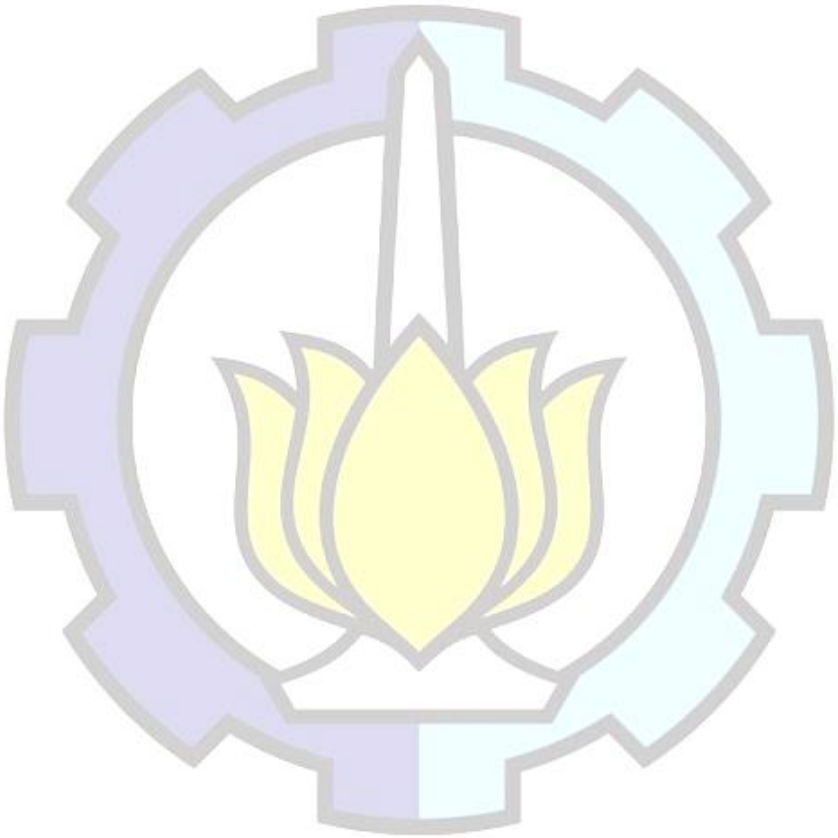
Gambar 4.8 Pengujian wireless charghing menggunakan metode fuzzy

Sebelum semua alat dinyalakan, pengecekan tiap sistem harus diuji kembali agar sistem keseluruhan berjalan dengan optimal. Ketika sistem dinyalakan maka akan terlihat gelombang input dan output pada osciloscope. Hasil pengujian sistem berupa arus pengisian baterai, temperatur baterai dan lama pengisian kemudian dicatat dan ditampilkan dengan grafik pada gambar 4.9 dibawah ini



Gambar 4.9. Grafik pengisian arus pada baterai terhadap waktu

Dari hasil grafik pengisian baterai dapat disimpulkan bahwa, selama proses pengisian baterai sistem akan memberikan nilai arusyang besar, hal ini bertujuan agar baterai cepat terisi. Pengisian ini akan terus berlanjut hingga 100 menit dan baterai mengalami kenaikan suhu karena kapasitas baterai telah terisi. Ketika suhu mulai naik, maka sistem fuzzy akan mengontrol tegangan input pada kumparan primer yang mengakibatkan arus masuk pada baterai berkurang saat pengisian. Sehingga arus akan berangsur-angsur turun hingga baterai terisi penuh. Sistem wireless



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BAB 5
KESIMPULAN DAN SARAN

5.1 Kesimpulan

Berdasarkan hasil pengujian dan analisa yang telah dilakukan, maka dapat disimpulkan sistem pengisian baterai nirkabel menggunakan metode fuzzy sebagai berikut:

1. Penggunaan modul AD9833 sebagai function generator dapat menghasilkan gelombang sinus hingga frekuensi 90 kHz bahkan lebih.
2. Perancangan frekuensi osilasi pada wireless charching tergantung pada nilai induktansi pada lilitan primer dan sekunder.
3. Metode fuzzy yang digunakan dapat mempercepat proses charging dan dapat mencegah baterai dari overheat saat charging.
4. Sistem rangkaian pengisi baterai menggunakan wireless charging memiliki efisiensi sekitar 80 % dengan jarak antar kumparan 1 cm.

5.2 Saran

Saran yang diberikan untuk pengembangan penelitian ini adalah:

1. Kesulitan yang dihadapi pada saat perancangan *hardware*, maka diperlukan analisis lebih lanjut terhadap desain function generator frekuensi tinggi yang digunakan, terutama pada kemampuan untuk menghasilkan frekuensi osilasi.
2. Penerapan sistem kontrol baru yang mampu menghasilkan proses perhitungan cepat pada sistem.

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Halaman ini sengaja dikosongkan

LAMPIRAN

```
//Program utama
#include <OneWire.h>
#include <DallasTemperature.h>

// sensor diletakkan di pin 8
#define ONE_WIRE_BUS 8

#define CS 2
#define UD 3
#define INC 4
const int analogPin= A0;

// setup sensor
OneWire oneWire(ONE_WIRE_BUS);

// berikan nama variabel,masukkan ke pustaka Dallas
DallasTemperature sensorSuhu(&oneWire);

unsigned long currentTime, prevTime;
const int ts = 50; //2 detik pengambilan smpling
float setpoint=50.0;
float suhu, arus, resistansi, defuz;

char buff[33];
int adcVal;
float Vadc;
unsigned int t;
```

```
float calib;

//kalman
const float var= 300;
float pc= 0;
float g= 0;
float p= 0;
float xp= 0;
float zp= 0;
float xe= 0;
float varProc= 50;

// masukkan nilai suhu dan arus
// nilai z = resistansi untuk digital potensio

// Fuzzifikasi
float f_suhu[5], f_arus[5];

// BISA DIGANTI-GANTI -> fuzifikasi suhu
float fs_N[2]  = {20, 25},
      fs_NS[3] = {20, 25, 30},
      fs_AZ[3] = {25, 30, 35},
      fs_PS[3] = {30, 35, 40},
      fs_P[2]  = {35, 40};

// BISA DIGANTI-GANTI -> fuzifikasi arus
float fa_N[2]  = {100, 200},
      fa_NS[3] = {100, 200, 300},
      fa_AZ[3] = {200, 300, 400},
```

```
    fa_PS[3] = {300, 400, 500},
    fa_P[2]  = {400, 500};

// Rule Base
float rule[5][5];

// BISA DIGANTI-GANTI -> resistansi
#define dN      -50.0  //-> kecil
#define dNS     -25.0  //-> agak kecil
#define dAZ       0.0  //-> sedang
#define dPS      25.0  //-> agak besar
#define dP       50.0 //-> besar

// BISA DIGANTI-GANTI -> Rule Base
float def_MOF[5][5] = {{ dP,  dP,  dPS, dAZ, dAZ},
                       { dP,  dPS, dAZ, dAZ, dAZ},
                       { dPS, dAZ, dAZ, dNS, dNS},
                       { dAZ, dNS, dNS, dNS, dNS},
                       { dNS, dNS, dNS, dN, dN}};

void fuzzifikasi(float in, float *out, float *T0, float *T1, float *T2, float *T3, float *T4){
  // N
  if(in < T0[0]){
    out[0] = 1;
  }
  else if(in >= T0[0] && in <= T0[1]){
    out[0] = (in - T0[1])/(T0[0] - T0[1]);
  }
```

```
else{
  out[0] = 0;
}

// NS
if(in < T1[0]){
  out[1] = 0;
}
else if(in >= T1[0] && in <= T1[1]){
  out[1] = (T1[0] - in)/(T1[0] - T1[1]);
}
else if(in >= T1[1] && in <= T1[2]){
  out[1] = (in - T1[2])/(T1[1] - T1[2]);
}
else{
  out[1] = 0;
}

// AZ
if(in < T2[0]){
  out[2] = 0;
}
else if(in >= T2[0] && in <= T2[1]){
  out[2] = (T2[0] - in)/(T2[0] - T2[1]);
}
else if(in >= T2[1] && in <= T2[2]){
  out[2] = (in - T2[2])/(T2[1] - T2[2]);
}
else{
```

```
  out[2] = 0;
 }

 //PS
 if(in < T3[0]){
  out[3] = 0;
 }
 else if(in >= T3[0] && in <= T3[1]){
  out[3] = (T3[0] - in)/(T3[0] - T3[1]);
 }
 else if(in >= T3[1] && in <= T3[2]){
  out[3] = (in - T3[2])/(T3[1] - T3[2]);
 }
 else{
  out[3] = 0;
 }

 // P
 if(in < T4[0]){
  out[4] = 0;
 }
 else if(in >= T4[0] && in <= T4[1]){
  out[4] = (T4[0] - in)/(T4[0] - T4[1]);
 }
 else{
  out[4] = 1;
 }
}
```

```
void ruleEvaluation(float *in1, float *in2, int index1, int index2){
  int i=0, j=0;
  float tempRule = 0;
  for(i=0;i<index1;i++){
    for(j=0;j<index2;j++){
      tempRule = min(in1[i], in2[j]);
      rule[i][j] = tempRule;
    }
  }
}

void defuzzifikasi(float &out, float *in1, float *in2, int index1, int index2){
    int i=0;
    float temp1 = 0, temp2 = 0;
    int cells = index1*index2;
    for(i=0;i<cells;i++){
      temp1 = temp1 + ((*(in1+i)) * (*(in2+i)));
    }
    i=0;
    for(i=0;i<cells;i++){
      temp2 = temp2 + *(in1+i);
    }
    out = temp1/temp2;
}

char datum = 0;

void setup(){
  t= millis();
```

```
  Serial.begin(9600);
  //saat kalibrasi sensor, jangan berikan input apa2 pada ACS
  kalibrasiSensor();

  sensorSuhu.begin();
  pinMode(CS, OUTPUT);
  pinMode(UD, OUTPUT);
  pinMode(INC, OUTPUT);
  resetPot();
  delay(500);
  prevTime = millis();
}

void loop(){
  currentTime = millis();
  if(currentTime - prevTime >= ts){
    suhu = ambilSuhu();
    //arus
    adcVal= analogRead(analogPin);
    //kalman
    pc= p+varProc;
    g= (float)(pc/(pc+var));
    p= (1-g)*pc;
    xp= xe;
    zp= xp;
    xe= g*(adcVal-zp)+xp;
    int adcValnew= xe;

    Vadc= ((float)5000*adcValnew/1023)-calib;
```

```
    arus= Vadc*10;
    if(arus<0)arus= 0;
    //arus= 200;

    fuzzifikasi(suhu,f_suhu,fs_N,fs_NS,fs_AZ,fs_PS,fs_P);
    fuzzifikasi(arus,f_arus,fa_N,fa_NS,fa_AZ,fa_PS,fa_P);
    ruleEvaluation(f_suhu,f_arus,5,5);
    defuzzifikasi(defuz,&rule[0][0],&def_MOF[0][0],5,5);
    resistansi = (int)round(defuz);
    if(resistansi<0){
      turun(resistansi);
    }
    else{
      naik(resistansi);
    }
    Serial.print("\nsuhu= ");
    Serial.print(suhu);
    Serial.print("  ADC arus= ");
    Serial.print(adcVal);
   // Serial.print(" arus= ");
   // Serial.println(arus);
    prevTime = currentTime;
  }
}

void resetPot (void){
  digitalWrite(INC,HIGH);
  digitalWrite(CS,LOW);
  digitalWrite(UD,LOW);
```

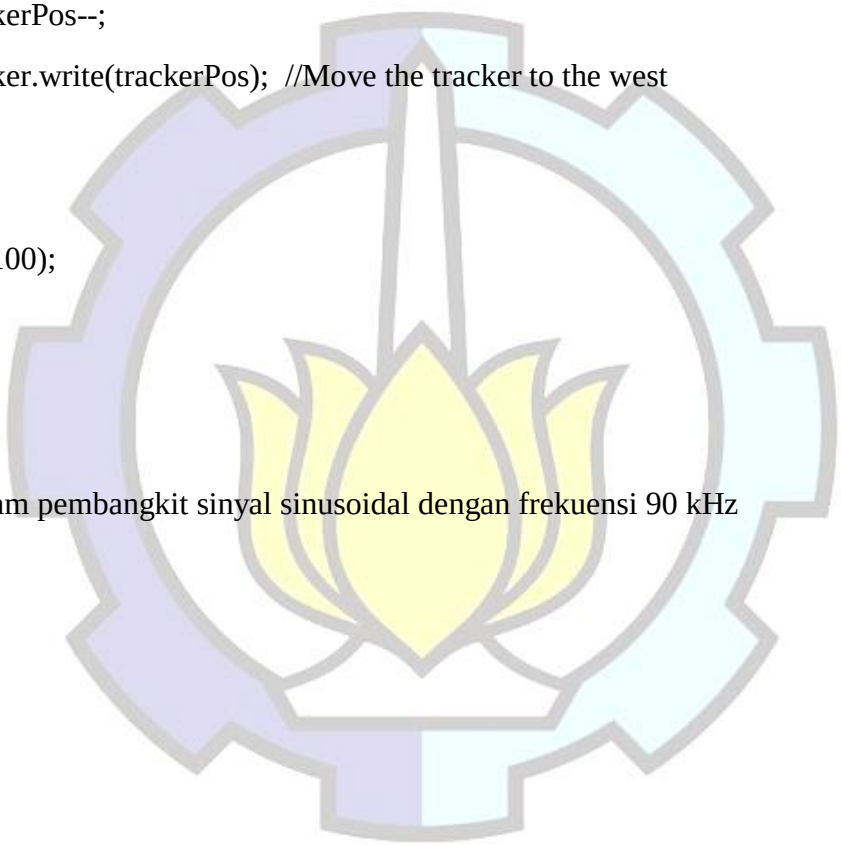
```
  for(char i=0;i<100;i++)
  {
    digitalWrite(INC, HIGH); // sets the pin on
    delayMicroseconds(5000); // pauses for 50 microseconds
    digitalWrite(INC, LOW); // sets the pin off
    delayMicroseconds(5000); // pauses for 50 microseconds
  }
  digitalWrite(INC,HIGH);
  digitalWrite(CS,HIGH);
  delay(50);
}

void Up(){
  digitalWrite(CS,LOW);
  digitalWrite(UD,HIGH);
  digitalWrite(INC,HIGH);

  delay(50);
  digitalWrite(INC,LOW);
  delay(50);
}

void Down(){
  digitalWrite(CS,LOW);
  digitalWrite(UD,LOW);
  digitalWrite(INC,HIGH);

  delay(50);
  digitalWrite(INC,LOW);
```

```
  delay(50);
}

void naik(int value){
  for(int i=0;i<abs(value);i++)
  {
    Up();
  }
  store();
}

void turun(int value){
  for(int i=0;i<abs(value);i++)
  {
    Down();
  }
  store();
}

void store(){
  digitalWrite(INC,HIGH);
  digitalWrite(CS,HIGH);
  delay(50);
  digitalWrite(CS,LOW);
}

float ambilSuhu(){
   sensorSuhu.requestTemperatures();
   float suhu = sensorSuhu.getTempCByIndex(0);
```

```
   return suhu;
}

void kalibrasiSensor(){
  for(int i=0;i<100;i++){
    adcVal= analogRead(analogPin);
    Vadc= (float)5000*adcVal/1023;
    calib+= Vadc;
    delay(100);
  }
  calib= (float)calib/100;
  Serial.println("proses kalibrasi selesai");
}

// Program tracking panel surya

#include <Servo.h>

Servo tracker;  // create servo object to control a servo
int eastLDRPin = 0;  //Assign analogue pins
int westLDRPin = 1;
int eastLDR = 0;   //Create variables for the east and west sensor values
int westLDR = 0;
int error = 0;
int calibration = 204;  //Calibration offset to set error to zero when both sensors receive an equal amount of light
int trackerPos = 90;    //Create a variable to store the servo position

void setup()
```

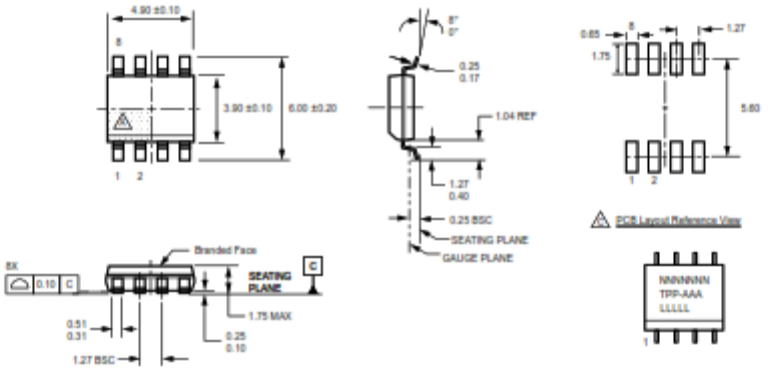
```
{
  tracker.attach(11);  // attaches the servo on pin 11 to the servo object
}



void loop()
{
  eastLDR = calibration + analogRead(eastLDRPin);    //Read the value of each of the east and west sensors
  westLDR = analogRead(westLDRPin);
  if(eastLDR<350 && westLDR<350)  //Check if both sensors detect very little light, night time
  {
    while(trackerPos<=160)  //Move the tracker all the way back to face east for sunrise
    {
      trackerPos++;
      tracker.write(trackerPos);
      delay(100);
    }
  }
  error = eastLDR - westLDR;          //Determine the difference between the two sensors.
  if(error>15)        //If the error is positive and greater than 15 then move the tracker in the east direction
  {
    if(trackerPos<=160)  //Check that the tracker is not at the end of its limit in the east direction
    {
      trackerPos++;
      tracker.write(trackerPos);  //Move the tracker to the east
```

```
    }
  }
  else if(error<-15)  //If the error is negative and less than -15 then move the tracker in the west direction
  {
    if(trackerPos>20)  //Check that the tracker is not at the end of its limit in the west direction
    {
      trackerPos--;
      tracker.write(trackerPos);  //Move the tracker to the west
    }
  }
  delay(100);
}
```



```
// Program pembangkit sinyal sinusoidal dengan frekuensi 90 kHz
```

Package LC, 8-pin SOIC



For Reference Only; not for tooling use (reference MS-012AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area
B Branding scale and appearance at supplier discretion
C Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

N = Device part number
T = Device temperature range
P = Package Designator
A = Amperage
L = Lot number
Belly Brand = Country of Origin

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Improving Sensing System Accuracy Using the FILTER Pin

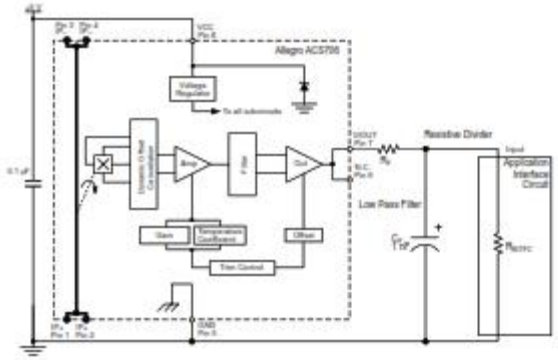
In low-frequency sensing applications, it is often advantageous to add a simple RC filter to the output of the device. Such a low-pass filter improves the signal-to-noise ratio, and therefore the resolution, of the device output signal. However, the addition of an RC filter to the output of a sensor IC can result in undesirable device output attenuation — even for DC signals.

Signal attenuation, ΔV_{ATT}, is a result of the resistive divider effect between the resistance of the external filter, R_F (see Application 6), and the input impedance and resistance of the customer interface circuit, R_{INTFC}. The transfer function of this resistive divider is given by:

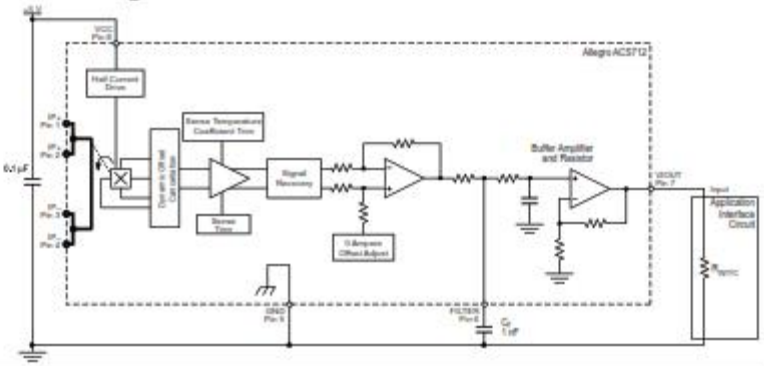
$$\Delta V_{ATT} = V_{IOUT}\left(\frac{R_{INTFC}}{R_F + R_{INTFC}}\right) .$$

Even if R_F and R_{INTFC} are designed to match, the two individual resistance values will most likely drift by different amounts over temperature. Therefore, signal attenuation will vary as a function of temperature. Note that, in many cases, the input impedance, R_{INTFC}, of a typical analog-to-digital converter (ADC) can be as low as 10 kΩ.

The ACS712 contains an internal resistor, a FILTER pin connection to the printed circuit board, and an internal buffer amplifier. With this circuit architecture, users can implement a simple RC filter via the addition of a capacitor, C_F (see Application 7) from the FILTER pin to ground. The buffer amplifier inside of the ACS712 (located after the internal resistor and FILTER pin connection) eliminates the attenuation caused by the resistive divider effect described in the equation for ΔV_{ATT}. Therefore, the ACS712 device is ideal for use in high-accuracy applications that cannot afford the signal attenuation associated with the use of an external RC low-pass filter.



Application 6. When a low pass filter is constructed externally to a standard Hall effect device, a resistive divider may exist between the filter resistor, R_F, and the resistance of the customer interface circuit, R_{INTFC}. This resistive divider will cause excessive attenuation, as given by the transfer function for ΔV_{ATT}.



Application 7. Using the FILTER pin provided on the ACS712 eliminates the attenuation effects of the resistor divider between R_F and R_{INTFC}, shown in Application 6.

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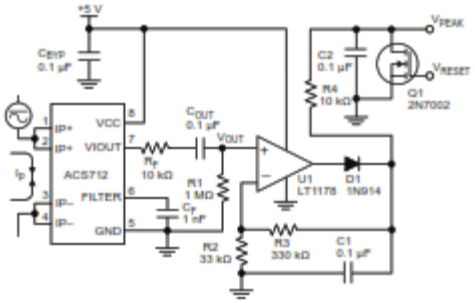
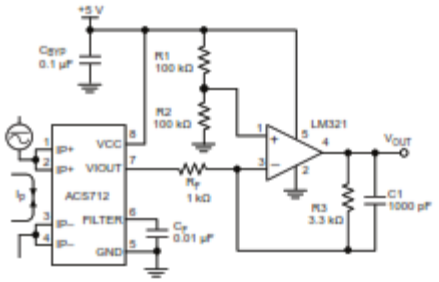
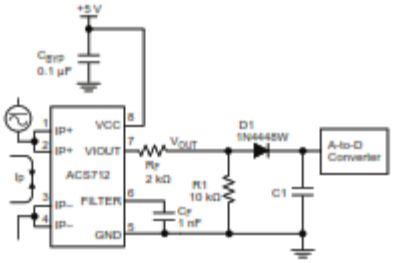
Typical Applications



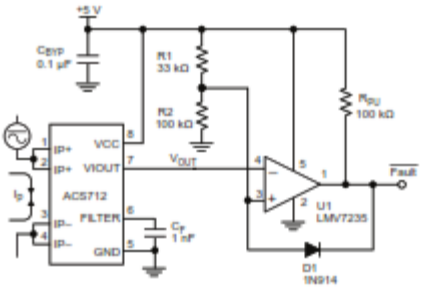
Application 2. Peak Detecting Circuit



Application 3. This configuration increases gain to 610 mV/A (tested using the ACS712ELC-05A).



Application 4. Rectified Output. 3.3 V scaling and rectification application for A-to-D converters. Replaces current transformer solutions with simpler ACS circuit. C1 is a function of the load resistance and filtering desired. R1 can be omitted if the full range is desired.



Application 5. 10 A Overcurrent Fault Latch. Fault threshold set by R1 and R2. This circuit latches an overcurrent fault and holds it until the 5 V rail is powered down.

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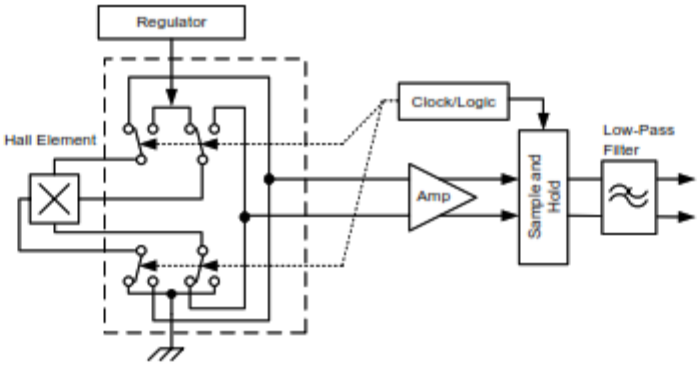
Chopper Stabilization Technique

Chopper Stabilization is an innovative circuit technique that is used to minimize the offset voltage of a Hall element and an associated on-chip amplifier. Allegro has a Chopper Stabilization technique that nearly eliminates Hall IC output drift induced by temperature or package stress effects. This offset reduction technique is based on a signal modulation-demodulation process. Modulation is used to separate the undesired DC offset signal from the magnetically induced signal in the frequency domain. Then, using a low-pass filter, the modulated DC offset is suppressed while the magnetically induced signal passes through the filter. As a result of this chopper stabilization approach, the output voltage from the Hall IC is desensitized to the effects of temperature and mechanical stress. This technique produces devices that have an extremely stable Electrical Offset Voltage, are immune to thermal stress, and have precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process that allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample and hold circuits.



Concept of Chopper Stabilization Technique

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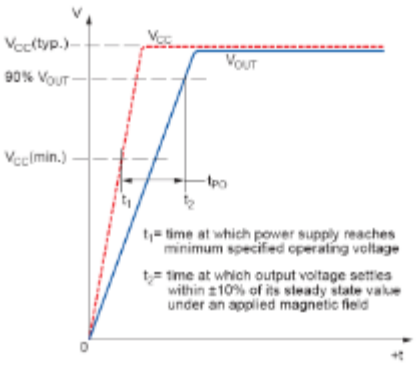
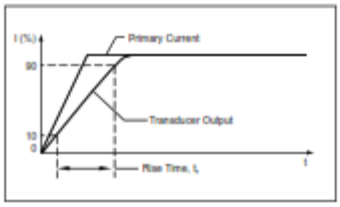
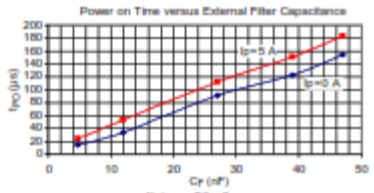
Definitions of Dynamic Response Characteristics

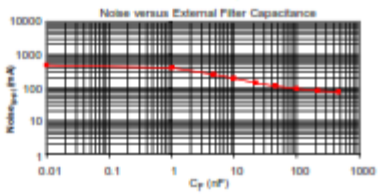
Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO} , is defined as the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.

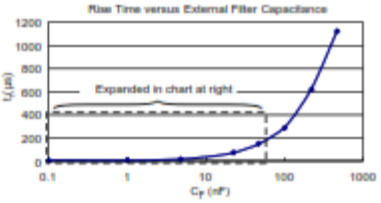


Rise time (t_r). The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the device, in which $f(-3\ dB) = 0.35 / t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

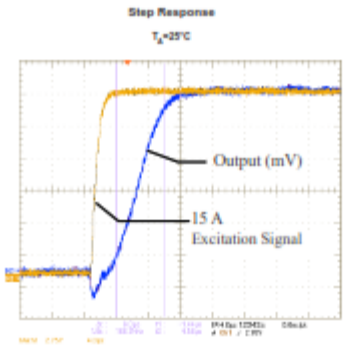


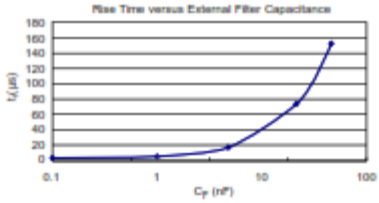






C_F (nF)	t_F (µs)
Open	3.5
1	5.8
4.7	17.5
22	73.5
47	88.2
100	291.3
220	623
470	1120





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Definitions of Accuracy Characteristics

Sensitivity (Sens). The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise (V_{NOISE}). The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC (≈1 G). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity (E_{LIN}). The degree to which the voltage output from the IC varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100\left\{1-\left[\frac{\Delta \text{ gain} \times \%\text{ sat}\,(V_{IOUT\_\text{full-scale amperes}} - V_{IOUT(Q)})}{2\,(V_{IOUT\_\text{half-scale amperes}} - V_{IOUT(Q)})}\right]\right\}$$

where $V_{IOUT\_\text{full-scale amperes}}$ = the output voltage (V) when the sampled current approximates full-scale $\pm I_P$.

Symmetry (E_{SYM}). The degree to which the absolute voltage output from the IC varies in proportion to either a positive or negative full-scale primary current. The following formula is used to derive symmetry:

$$100\left(\frac{V_{IOUT\_+\text{ full-scale amperes}} - V_{IOUT(Q)}}{V_{IOUT(Q)} - V_{IOUT\_-\text{full-scale amperes}}}\right)$$

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the device when the primary current is zero. For a unipolar supply voltage, it nominally remains at $V_{CC}/2$. Thus, V_{CC} = 5 V translates into $V_{IOUT(Q)}$ = 2.5 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent value of $V_{CC}/2$ due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Accuracy (E_{TOT}). The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total output error. The accuracy is illustrated graphically in the output voltage versus current chart at right.

Accuracy is divided into four areas:

- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy at the zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy at the the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over Δ temperature.** Accuracy at the full-scale current flow including temperature effects.

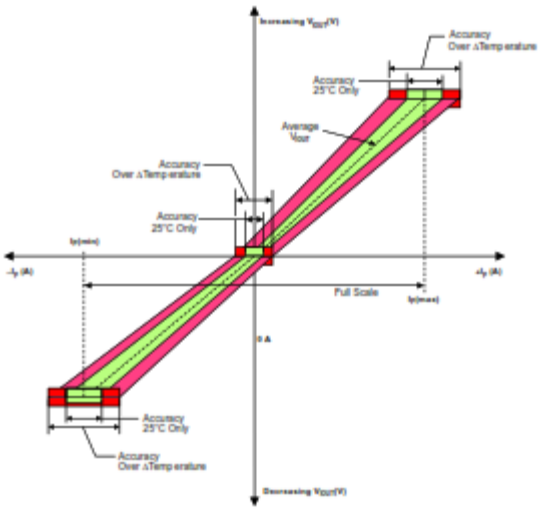
Ratiometry. The ratiometric feature means that its 0 A output, $V_{IOUT(Q)}$, (nominally equal to $V_{CC}/2$) and sensitivity, Sens, are proportional to its supply voltage, V_{CC}. The following formula is used to derive the ratiometric change in 0 A output voltage, $\Delta V_{IOUT(Q)RAT}$ (%).

$$100\left(\frac{V_{IOUT(Q)VCC} / V_{IOUT(Q)5V}}{V_{CC} / 5\text{ V}}\right)$$

The ratiometric change in sensitivity, $\Delta Sens_{RAT}$ (%), is defined as:

$$100\left(\frac{Sens_{VCC} / Sens_{5V}}{V_{CC} / 5\text{ V}}\right)$$

Output Voltage versus Sampled Current
Accuracy at 0 A and at Full-Scale Current



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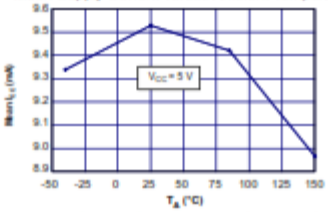
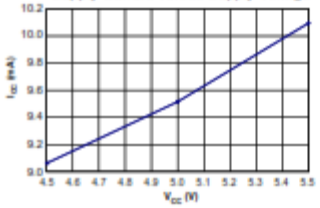
Characteristic Performance

I_P = 30 A, unless otherwise specified

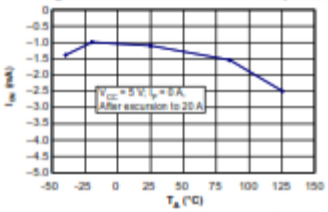
Mean Supply Current versus Ambient Temperature



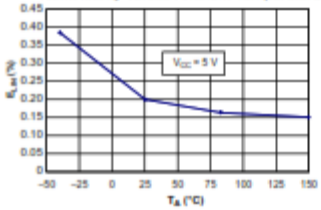
Supply Current versus Supply Voltage



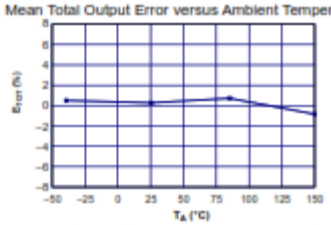
Magnetic Offset versus Ambient Temperature



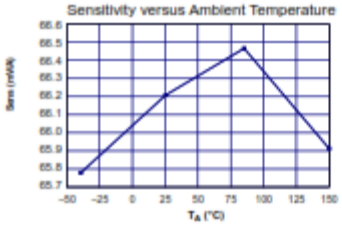
Nonlinearity versus Ambient Temperature



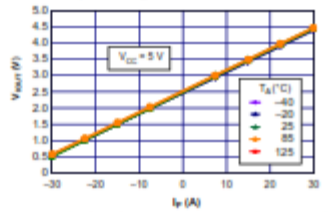
Mean Total Output Error versus Ambient Temperature



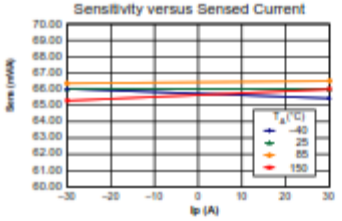
Sensitivity versus Ambient Temperature



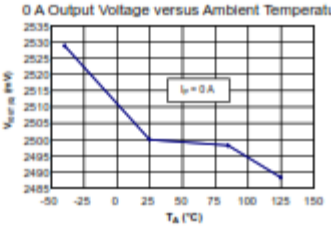
Output Voltage versus Sensed Current



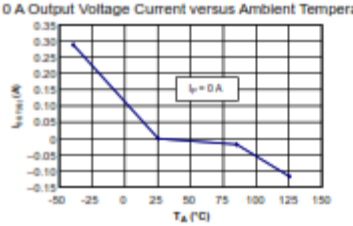
Sensitivity versus Sensed Current



0 A Output Voltage versus Ambient Temperature



0 A Output Voltage Current versus Ambient Temperature



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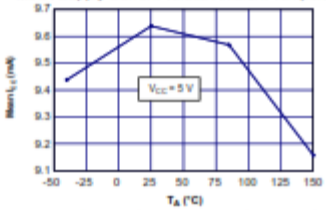
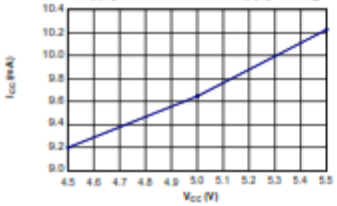
Characteristic Performance

I_P = 20 A, unless otherwise specified

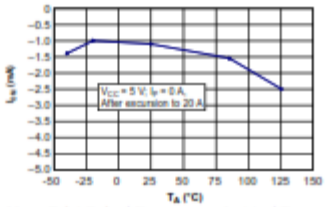
Mean Supply Current versus Ambient Temperature



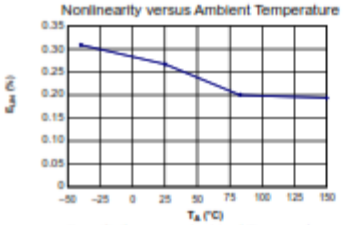
Supply Current versus Supply Voltage



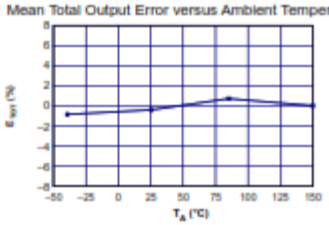
Magnetic Offset versus Ambient Temperature



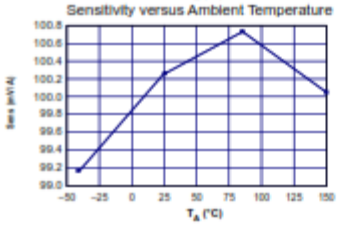
Nonlinearity versus Ambient Temperature



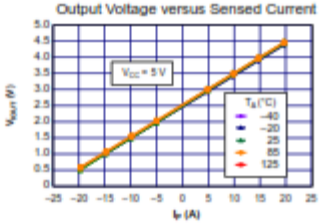
Mean Total Output Error versus Ambient Temperature



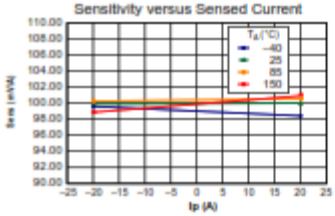
Sensitivity versus Ambient Temperature



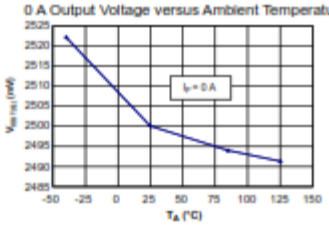
Output Voltage versus Sensed Current



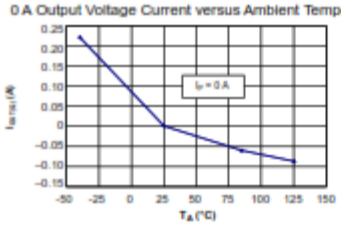
Sensitivity versus Sensed Current



0 A Output Voltage versus Ambient Temperature



0 A Output Voltage Current versus Ambient Temperature



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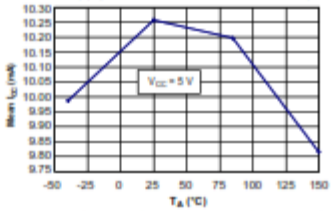
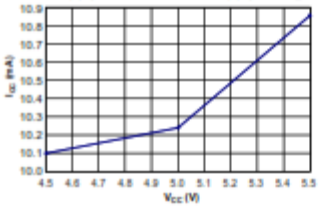
Characteristic Performance

I_P = 5 A, unless otherwise specified

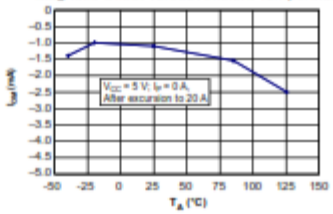
Mean Supply Current versus Ambient Temperature



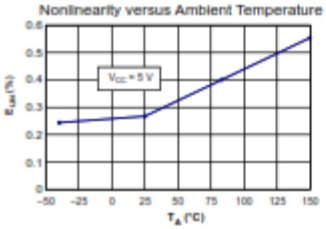
Supply Current versus Supply Voltage



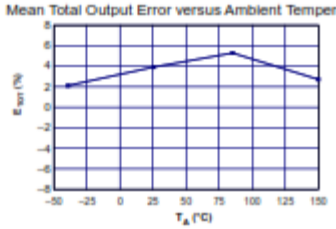
Magnetic Offset versus Ambient Temperature



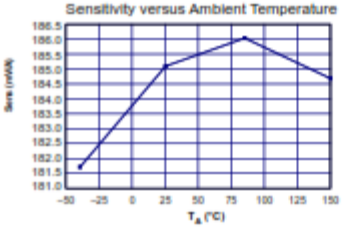
Nonlinearity versus Ambient Temperature



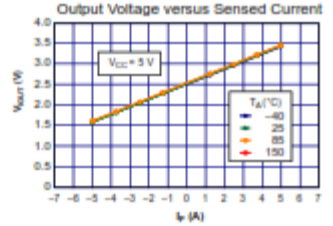
Mean Total Output Error versus Ambient Temperature



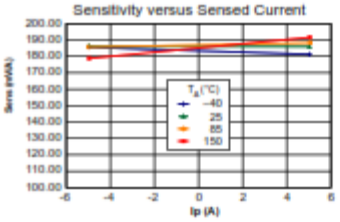
Sensitivity versus Ambient Temperature



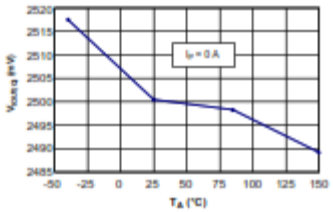
Output Voltage versus Sensed Current



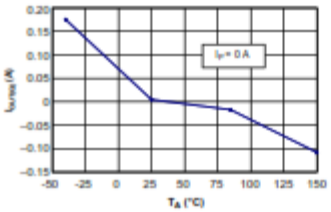
Sensitivity versus Sensed Current



0 A Output Voltage versus Ambient Temperature



0 A Output Voltage Current versus Ambient Temperature



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x05B PERFORMANCE CHARACTERISTICS[1] T_A = –40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–5	–	5	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	180	185	190	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 185 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	21	–	mV
Zero Current Output Slope	$\Delta V_{OUT(Q)}$	T_A = –40°C to 25°C	–	–0.26	–	mV/°C
		T_A = 25°C to 150°C	–	–0.05	–	mV/°C
Sensitivity Slope	ΔSens	T_A = –40°C to 25°C	–	0.054	–	mV/A/°C
		T_A = 25°C to 150°C	–	–0.006	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P = ±5 A, T_A = 25°C	–	±1.5	–	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, $T_{J(max)}$, is not exceeded.

[2]Percentage of I_P, with I_P = 5 A. Output filtered.

x20A PERFORMANCE CHARACTERISTICS[1] T_A = –40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–20	–	20	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	96	100	104	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 100 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	11	–	mV
Zero Current Output Slope	$\Delta V_{OUT(Q)}$	T_A = –40°C to 25°C	–	–0.34	–	mV/°C
		T_A = 25°C to 150°C	–	–0.07	–	mV/°C
Sensitivity Slope	ΔSens	T_A = –40°C to 25°C	–	0.017	–	mV/A/°C
		T_A = 25°C to 150°C	–	–0.004	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P = ±20 A, T_A = 25°C	–	±1.5	–	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]Percentage of I_P, with I_P = 20 A. Output filtered.

x30A PERFORMANCE CHARACTERISTICS[1] T_A = –40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–30	–	30	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	63	66	69	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 66 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	7	–	mV
Zero Current Output Slope	$\Delta V_{OUT(Q)}$	T_A = –40°C to 25°C	–	–0.35	–	mV/°C
		T_A = 25°C to 150°C	–	–0.05	–	mV/°C
Sensitivity Slope	ΔSens	T_A = –40°C to 25°C	–	0.007	–	mV/A/°C
		T_A = 25°C to 150°C	–	–0.002	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P = ±30 A, T_A = 25°C	–	±1.5	–	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]Percentage of I_P, with I_P = 30 A. Output filtered.

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COMMON OPERATING CHARACTERISTICS[1] over full range of T_A, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	V_{CC} = 5.0 V, output open	–	10	13	mA
Output Capacitance Load	C_{LOAD}	VIOUT to GND	–	–	10	nF
Output Resistive Load	R_{LOAD}	VIOUT to GND	4.7	–	–	kΩ
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	1.2	–	mΩ
Rise Time	t_r	I_P = I_P(max), T_A = 25°C, C_{OUT} = open	–	3.5	–	µs
Frequency Bandwidth	f	–3 dB, T_A = 25°C; I_P is 10 A peak-to-peak	–	80	–	kHz
Nonlinearity	E_{LIN}	Over full range of I_P	–	1.5	–	%
Symmetry	E_{SYM}	Over full range of I_P	98	100	102	%
Zero Current Output Voltage	$V_{IOUT(Q)}$	Bidirectional; I_P = 0 A, T_A = 25°C	–	V_{CC} × 0.5	–	V
Power-On Time	t_{PO}	Output reaches 90% of steady-state level, T_J = 25°C, 20 A present on leadframe	–	35	–	µs
Magnetic Coupling[2]			–	12	–	G/A
Internal Filter Resistance[3]	$R_{F(INT)}$			1.7		kΩ

[1]Device may be operated at higher primary current levels, I_P, and ambient, T_A, and internal leadframe temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]1G = 0.1 mT.

[3]$R_{F(INT)}$ forms an RC circuit via the FILTER pin.

COMMON THERMAL CHARACTERISTICS[1]

			Min.	Typ.	Max.	Units
Operating Internal Leadframe Temperature	T_A	E range	–40	–	85	°C
					Value	Units
Junction-to-Lead Thermal Resistance[2]	$R_{\theta JL}$	Mounted on the Allegro ASEK 712 evaluation board			5	°C/W
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	Mounted on the Allegro 85-0322 evaluation board, includes the power consumed by the board			23	°C/W

[1]Additional thermal information is available on the Allegro website.

[2]The Allegro evaluation board has 1500 mm² of 2 oz. copper on each side, connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Performance values include the power consumed by the PCB. Further details on the board are available from the Frequently Asked Questions document on our website. Further information about board design and thermal performance also can be found in the Applications Information section of this datasheet.

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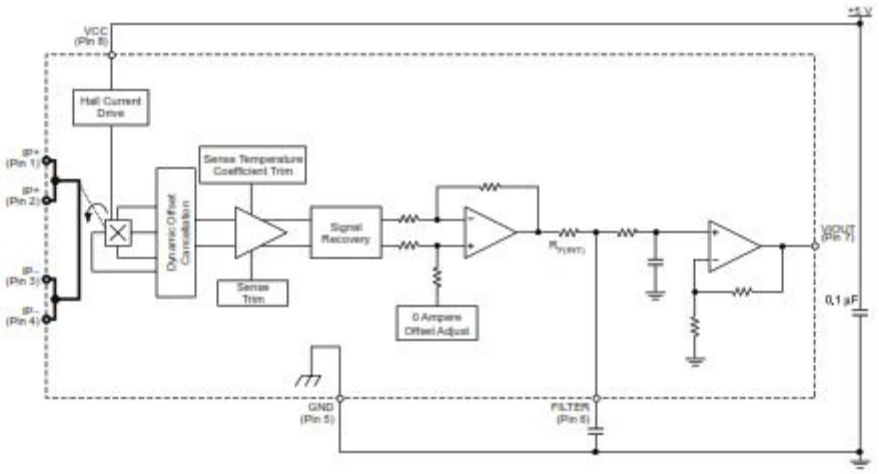
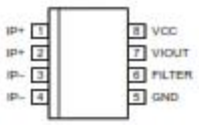
Functional Block Diagram



Pin-out Diagram



Terminal List Table

Number	Name	Description
1 and 2	IP+	Terminals for current being sampled; fused internally
3 and 4	IP–	Terminals for current being sampled; fused internally
5	GND	Signal ground terminal
6	FILTER	Terminal for external capacitor that sets bandwidth
7	VIOUT	Analog output signal
8	VCC	Device power supply terminal

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Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Description (continued)

the device at up to 5× overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads (pins 5 through 8). This allows the ACS712 to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The ACS712 is provided in a small, surface mount SOIC8 package. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

Selection Guide

Part Number	Packing*	T_A (°C)	Optimized Range, I_p (A)	Sensitivity, Sens (Typ) (mV/A)
ACS712ELCTR-05B-T	Tape and reel, 3000 pieces/reel	–40 to 85	±5	185
ACS712ELCTR-20A-T	Tape and reel, 3000 pieces/reel	–40 to 85	±20	100
ACS712ELCTR-30A-T	Tape and reel, 3000 pieces/reel	–40 to 85	±30	66

*Contact Allegro for additional packing options.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Output Voltage	V_{IOUT}		8	V
Reverse Output Voltage	V_{RIOUT}		–0.1	V
Output Current Source	$I_{IOUT(Source)}$		3	mA
Output Current Sink	$I_{IOUT(Sink)}$		10	mA
Overcurrent Transient Tolerance	I_p	1 pulse, 100 ms	100	A
Nominal Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Isolation Characteristics

Characteristic	Symbol	Notes	Rating	Unit
Dielectric Strength Test Voltage*	V_{ISO}	Agency type-tested for 60 seconds per UL standard 60950-1, 1st Edition	2100	VAC
Working Voltage for Basic Isolation	V_{WFSI}	For basic (single) isolation per UL standard 60950-1, 1st Edition	354	VDC or V_{pk}
Working Voltage for Reinforced Isolation	V_{WFRI}	For reinforced (double) isolation per UL standard 60950-1, 1st Edition	184	VDC or V_{pk}

* Allegro does not conduct 60-second testing. It is done only during the UL certification process.

Parameter	Specification
Fire and Electric Shock	CAN/CSA-C22.2 No. 60950-1-03 UL 60950-1:2003 EN 60950-1:2001

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ACS712

Fully Integrated, Hall-Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor

Features and Benefits

- Low-noise analog signal path
- Device bandwidth is set via the new FILTER pin
- 5 µs output rise time in response to step input current
- 80 kHz bandwidth
- Total output error 1.5% at T_A = 25°C
- Small footprint, low-profile SOIC8 package
- 1.2 mΩ internal conductor resistance
- 2.1 kVRMS minimum isolation voltage from pins 1-4 to pins 5-8
- 5.0 V, single supply operation
- 66 to 185 mV/A output sensitivity
- Output voltage proportional to AC or DC currents
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Nearly zero magnetic hysteresis
- Ratiometric output from supply voltage

TÜV America
Certificate Number:
U8V 15 05 54214 038
CB 13 08 54214 026

Package: 8-Lead SOIC (suffix LC)

Not to scale

Description

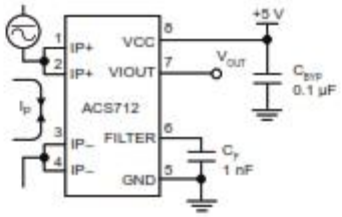
The Allegro™ ACS712 provides economical and precise solutions for AC or DC current sensing in industrial, commercial, and communications systems. The device package allows for easy implementation by the customer. Typical applications include motor control, load detection and management, switch-mode power supplies, and overcurrent fault protection. The device is not intended for automotive applications.

The device consists of a precise, low-offset, linear Hall circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy after packaging.

The output of the device has a positive slope (>$V_{IOUT(Q)}$) when an increasing current flows through the primary copper conduction path (from pins 1 and 2, to pins 3 and 4), which is the path used for current sampling. The internal resistance of this conductive path is 1.2 mΩ typical, providing low power loss. The thickness of the copper conductor allows survival of

Continued on the next page…

Typical Application



Application 1. The ACS712 outputs an analog signal, V_{OUT}, that varies linearly with the uni- or bi-directional AC or DC primary sampled current, I_P, within the range specified. C_F is recommended for noise management, with values that depend on the application.

Revision History

Number	Date	Description
15	November 16, 2012	Update rise time and isolation, I_{OUT} reference data, patents
16	June 5, 2017	Updated product status
17	December 10, 2018	Updated certificate numbers
18	May 17, 2019	Updated TUV certificate mark, and minor editorial updates

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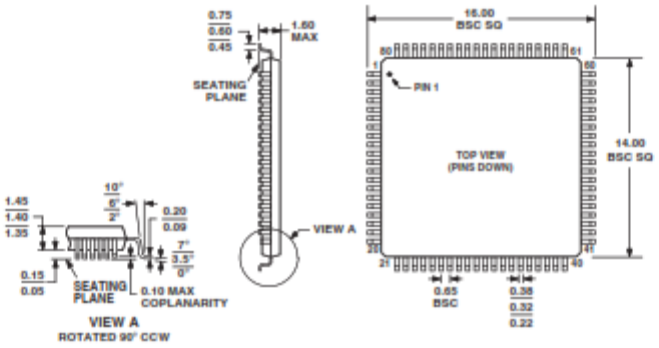
Revision History

Location	Page
8/03—Data Sheet changed from REV. A to REV. B.	
Added B Grade models	Universal
Edits to SPECIFICATIONS	2
Change to ABSOLUTE MAXIMUM RATINGS	6
Changes to ORDERING GUIDE	6
Replaced Table II	12
Edits to Table V	13
Edits to Table VI	16
Edits to Sync-on-Green Slicer Threshold section	20
Edits to Table XXXI	21
Edits to 4:2:2 Output Mode Select section	22
Edits to Sync Separator section	24
Edits to Outputs section	25
Updated OUTLINE DIMENSIONS	26
5/02—Data Sheet changed from REV. 0 to REV. A.	
Edits to SPECIFICATIONS	2
Edits to PIN CONFIGURATION	5
Edits to Table II	10
Edits to Clock Generation section	10
Edits to Figure 8 and Figure 9	12
Edits to Table VI	13
Edits to Table VII	15
Edits to CLAMP TIMING section	16
Edits to Table XIV	17
Edits to Clamp Input Signal Polarity section	17
Edits to 4:2:2 Output Mode Select section	20
Edits to Table XXXV	20
Edits to 2-WIRE SERIAL CONTROL PORT section	20

OUTLINE DIMENSIONS

80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80)
Dimensions shown in millimeters



It is also recommended to use a single ground plane for the entire board. Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommended to at least place a single ground plane under the AD9883A. The location of the split should be at the receiver of the digital outputs. For this case it is even more important to place components wisely because the current loops will be much longer (current takes the path of least resistance). An example of a current loop:

Figure 13. Current Loop

PLL
Place the PLL loop filter components as close to the FILT pin as possible.

Do not place any digital or other high frequency traces near these components.

Use the values suggested in the data sheet with 10% tolerances or less.

Outputs (Both Data and Clocks)
Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, which requires more current, which causes more internal digital noise.

Shorter traces reduce the possibility of reflections.

Adding a series resistor of value 22 Ω to 100 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside of the AD9883A. However, if 50 Ω traces are used on the PCB, the data outputs should not need resistors. A 22 Ω resistor on the DATACK output should provide good impedance matching that will reduce reflections. If series resistors are used, place them as close to the AD9883A pins as possible (although try not to add vias or extra length to the output trace in order to get the resistors closer).

If possible, limit the capacitance that each of the digital outputs drives to less than 10 pF. This can easily be accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance will increase the current transients inside of the AD9883A, creating more digital noise on its power supplies.

Digital Inputs
The digital inputs on the AD9883A were designed to work with 3.3 V signals, but are tolerant of 5.0 V signals. Therefore, no extra components need to be added if using 5.0 V logic.

Any noise that gets onto the Hsync input trace will add jitter to the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

Voltage Reference
Bypass with a 0.1 µF capacitor. Place as close to the AD9883A pin as possible. Make the ground connection as short as possible.

Table XXXVIII. Control of the Sync Block Muxes via the Serial Register

Mux No.	Serial Bus Control Bit	Control Bit State	Result
1 and 2	0EH: Bit 3	0	Pass Hsync
		1	Pass Sync-on-Green
3	0FH: Bit 5	0	Pass Coast
		1	Pass Vsync
4	0EH: Bit 0	0	Pass Vsync
		1	Pass Sync Separator Signal

Sync Slicer

The purpose of the sync slicer is to extract the sync signal from the Green graphics channel. A sync signal is not present on all graphics systems, only those with Sync-on-Green. The sync signal is extracted from the Green channel in a two-step process. First, the SOG input is clamped to its negative peak (typically 0.3 V below the black level). Next, the signal goes to a comparator with a variable trigger level, nominally 0.15 V above the clamped level. The "sliced" sync is typically a composite sync signal containing both Hsync and Vsync.

Sync Separator

A sync separator extracts the Vsync signal from a composite sync signal. It does this through a low-pass filter-like or integrator-like operation. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal, so it rejects any signal shorter than a threshold value, which is somewhere between an Hsync pulsewidth and a Vsync pulsewidth.

The sync separator on the AD9883A is simply an 8-bit digital counter with a 5 MHz clock. It works independently of the polarity of the composite sync signal. (Polarities are determined elsewhere on the chip.) The basic idea is that the counter counts up when Hsync pulses are present. But since Hsync pulses are relatively short in width, the counter only reaches a value of N before the pulse ends. It then starts counting down eventually reaching 0 before the next Hsync pulse arrives. The specific value of N will vary for different video modes, but will always be less than 255. For example with a 1 µs width Hsync, the counter will only reach 5 (1 µs/200 ns = 5). Now, when Vsync is present on the composite sync the counter will also count up. However, since the Vsync signal is much longer, it will count to a higher number M. For most video modes, M will be at least 255. So, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection (T) can be programmed through the serial register (11H).

Once Vsync has been detected, there is a similar process to detect when it goes inactive. At detection, the counter first resets to 0, then starts counting up when Vsync goes away. Similar to the previous case, it will detect the absence of Vsync when the counter reaches the threshold count (T). In this way, it will reject noise and/or serration pulses. Once Vsync is detected to be absent, the counter resets to 0 and begins the cycle again.

PCB LAYOUT RECOMMENDATIONS

The AD9883A is a high precision, high speed analog device. As such, to get the maximum performance out of the part, it is important to have a well laid out board. The following is a guide for designing a board using the AD9883A.

Analog Interface Inputs

Using the following layout techniques on the graphics inputs is extremely important.

Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9883A as close as possible to the graphics VGA connector. Long input trace lengths are undesirable because they pick up more noise from the board and other external sources.

Place the 75 Ω termination resistors (see Figure 1) as close to the AD9883A chip as possible. Any additional trace length between the termination resistors and the input of the AD9883A increases the magnitude of reflections, which will corrupt the graphics signal.

Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω will also increase the chance of reflections.

The AD9883A has very high input bandwidth (500 MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it will also capture any high frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. Avoid running any digital traces near the analog inputs.

Due to the high bandwidth of the AD9883A, low-pass filtering the analog inputs can sometimes help to reduce noise. (For many applications, filtering is unnecessary.) Experiments have shown that placing a series ferrite bead prior to the 75 Ω termination resistor is helpful in filtering out excess noise. Specifically, the part used was the #2508051217Z0 from Fair-Rite, but each application may work best with a different bead value. Alternately, placing a 100 Ω to 120 Ω resistor between the 75 Ω termination resistor and the input coupling capacitor can also be beneficial.

Power Supply Bypassing

It is recommended to bypass each power supply pin with a 0.1 µF capacitor. The exception is when two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is necessary to have only one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9883A, as that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PV_D (the clock generator supply). Abrupt changes in PV_D can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (V_D and PV_D).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PV_D, from a different, cleaner power source (for example, from a 12 V supply).

Data is read from the control registers of the AD9883A in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/$\overline{W}$ Bit of the slave address byte low to set up a sequential read operation.

Reading (the R/$\overline{W}$ Bit of the slave address byte high) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the AD9883A, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to one control register
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = Low)
- Base Address Byte
- Data Byte to Base Address
- Stop Signal

Write to four consecutive control registers
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = Low)
- Base Address Byte
- Data Byte to Base Address
- Data Byte to (Base Address + 1)
- Data Byte to (Base Address + 2)
- Data Byte to (Base Address + 3)
- Stop Signal

Read from one control register
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = Low)
- Base Address Byte
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = High)
- Data Byte from Base Address
- Stop Signal

Read from four consecutive control registers
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = Low)
- Base Address Byte
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = High)
- Data Byte from Base Address
- Data Byte from (Base Address + 1)
- Data Byte from (Base Address + 2)
- Data Byte from (Base Address + 3)
- Stop Signal

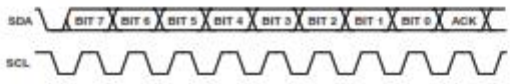


Figure 11. Serial Interface—Typical Byte Transfer

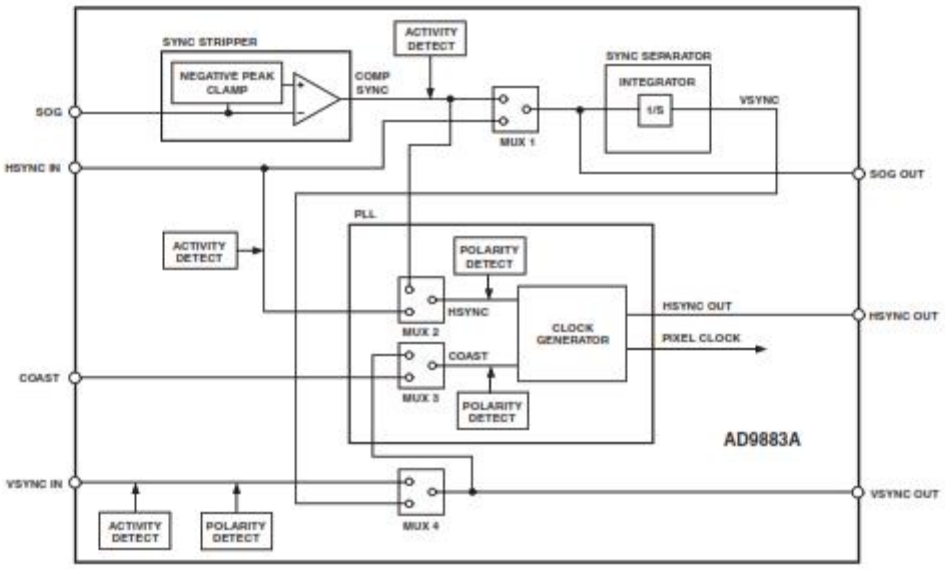


Figure 12. Sync Processing Block Diagram

Table XXXIV. Detected Coast Input Polarity Status

Polarity Status	Result
0	Coast Polarity Negative
1	Coast Polarity Positive

This indicates that Bit 1 of Register 5 is the 4:2:2 Output mode select bit.

15 1 **4:2:2 Output Mode Select**
A bit that configures the output data in 4:2:2 mode. This mode can be used to reduce the number of data lines used from 24 down to 16 for applications using YUV, YCbCr, or YPbPr graphics signals. A timing diagram for this mode is shown in Figure 9.

Recommended input and output configurations are shown in Table XXXV.

Table XXXV. 4:2:2 Output Mode Select

Select	Output Mode
0	4:2:2
1	4:4:4

Table XXXVI. 4:2:2 Input/Output Configuration

Channel	Input Connection	Output Format
Red	V	U/V
Green	Y	Y
Blue	U	High Impedance

2-WIRE SERIAL CONTROL PORT
A 2-wire serial interface control interface is provided. Up to two AD9883A devices may be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are five components to serial bus operation:

- Start Signal
- Slave Address Byte
- Base Register Address Byte
- Data Byte to Read or Write
- Stop Signal

When the serial interface is inactive (SCL and SDA are high) communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a 7-bit slave address (the first seven bits) and a single R/$\overline{W}$ Bit (the eighth bit). The R/$\overline{W}$ Bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA_{1-0} input pins in Table XXXIV, the AD9883A acknowledges by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the AD9883A does not acknowledge.

Table XXXVII. Serial Port Addresses

Bit 7 A_6 (MSB)	Bit 6 A_5	Bit 5 A_4	Bit 4 A_3	Bit 3 A_2	Bit 2 A_1	Bit 1 A_0
1	0	0	1	1	0	0
1	0	0	1	1	0	1

Data Transfer via Serial Interface
For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9883A does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9883A during a read sequence, the AD9883A interprets this as "end of data." The SDA remains high so the master can generate a stop signal.

Writing data to specific control registers of the AD9883A requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remains at its maximum value of 14H. Any base address higher than 14H will not produce an acknowledge signal.

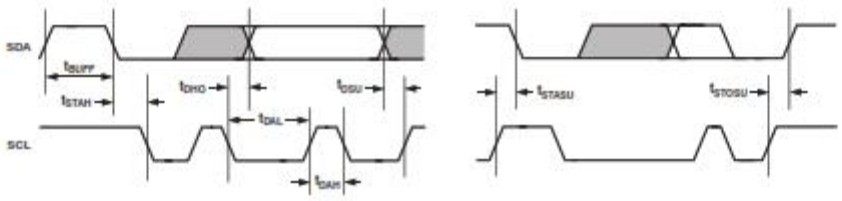


Figure 10. Serial Port Read/Write Timing

13 **7–0 Post-Coast**
This register allows the coast signal to be applied following the Vsync signal. This is necessary in cases where post-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

14 **7 Hsync Detect**
This bit is used to indicate when activity is detected on the Hsync input pin (Pin 30). If Hsync is held high or low, activity will not be detected.

Table XXVII. Hsync Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The sync processing block diagram shows where this function is implemented.

14 **6 AHS – Active Hsync**
This bit indicates which Hsync input source is being used by the PLL (Hsync input or Sync-on-Green). Bits 7 and 1 in this register determine which source is used. If both Hsync and SOG are detected, the user can determine which has priority via Bit 3 in register 0EH. The user can override this function via Bit 4 in register 0EH. If the override bit is set to Logic 1, then this bit will be forced to whatever the state of Bit 3 in register 0EH is set to.

Table XXVIII. Active Hsync Results

Bit 7 (Hsync Detect)	Bit 1 (SOG Detect)	Bit 4, Reg 0EH (Override)	AHS
0	0	0	Bit 3 in 0EH
0	1	0	1
1	0	0	0
1	1	0	Bit 3 in 0EH
X	X	1	Bit 3 in 0EH

AHS = 0 means use the Hsync pin input for Hsync.
AHS = 1 means use the SOG pin input for Hsync.

The override bit is in register 0EH, Bit 4.

14 **5 Detected Hsync Input Polarity Status**
This bit reports the status of the Hsync input polarity detection circuit. It can be used to determine the polarity of the Hsync input. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 12).

Table XXIX. Detected Hsync Input Polarity Status

Hsync Polarity Status	Result
0	Negative
1	Positive

14 **4 Vsync Detect**
This bit is used to indicate when activity is detected on the Vsync input pin (Pin 31). If Vsync is held steady high or low, activity will not be detected.

Table XXX. Vsync Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The Sync Processing Block Diagram (Figure 12) shows where this function is implemented.

14 **3 AVS – Active Vsync**
This bit indicates which Vsync source is being used: the Vsync input or output from the sync separator. Bit 4 in this register determines which is active. If both Vsync and SOG are detected, the user can determine which has priority via Bit 0 in register 0EH. The user can override this function via Bit 1 in register 0EH. If the override bit is set to Logic 1, this bit will be forced to whatever the state of Bit 0 in register 0EH is set.

Table XXXI. Active Vsync Results

Bit 4, Reg 14H (Vsync Detect)	Bit 1, Reg 0EH (Override)	AVS
1	0	0
0	0	1
X	1	Bit 0 in 0EH

AVS = 0 means Vsync input.
AVS = 1 means Sync separator.

The override bit is in register 0EH, Bit 1.

14 **2 Detected Vsync Output Polarity Status**
This bit reports the status of the Vsync output polarity detection circuit. It can be used to determine the polarity of the Vsync output. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 12).

Table XXXII. Detected Vsync Output Polarity Status

Vsync Polarity Status	Result
0	Active Low
1	Active High

14 **1 Sync-on-Green Detect**
This bit is used to indicate when sync activity is detected on the Sync-on-Green input pin (Pin 49).

Table XXXIII. Sync-on-Green Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The Sync Processing Block Diagram (Figure 12) shows where this function is implemented.

14 **0 Detected Coast Polarity Status**
This bit reports the status of the Coast input polarity detection circuit. It can be used to determine the polarity of the Coast input. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 12).

0F 4 **Coast Input Polarity Override**
This register is used to override the internal circuitry that determines the polarity of the Coast signal going into the PLL.

Table XX. Coast Input Polarity Override Settings

Override Bit	Result
0	Determined by Chip
1	Determined by User

The default for coast polarity override is 0.

0F 3 **Coast Input Polarity**
This bit indicates the polarity of the Coast signal that is applied to the PLL COAST input.

Table XXI. Coast Input Polarity Settings

Coast Polarity	Function
0	Active Low
1	Active High

Active Low means that the clock generator will ignore Hsync inputs when Coast is low, and continue operating at the same nominal frequency until Coast goes high.

Active High means that the clock generator will ignore Hsync inputs when Coast is high, and continue operating at the same nominal frequency until Coast goes low.

This function needs to be used along with the Coast Polarity Override bit (Bit 4).

The power-up default value is 1.

0F 2 **Seek Mode Override**
This bit is used to either allow or disallow the low power mode. The low power mode (Seek Mode) occurs when there are no signals on any of the Sync inputs.

Table XXII. Seek Mode Override Settings

Select	Result
1	Allow Seek Mode
0	Disallow Seek Mode

The default for this register is 1.

0F 1 **PWRDN**
This bit is used to put the chip in full power-down. See Power Management Section for details of which blocks are powered down.

Table XXIII. Power-Down Settings

Select	Result
0	Power-Down
1	Normal Operation

The default for this register is 1.

10 7-3 **Sync-on-Green Slicer Threshold**
This register allows the comparator threshold of the Sync-on-Green slicer to be adjusted. This register adjusts it in steps of 10 mV, with the minimum setting equaling 10 mV (11111) and the maximum setting equaling 330 mV (00000). The default setting is 23, which corresponds to a threshold value of 100 mV; for a threshold of 150 mV, the setting should be 18.

10 2 **Red Clamp Select**
This bit determines whether the Red channel is clamped to ground or to midscale. For RGB video, all three channels are referenced to ground. For YCbCr (or YUV), the Y channel is referenced to ground, but the CbCr channels are referenced to midscale. Clamping to midscale actually clamps to Pin 37.

Table XXIV. Red Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 37)

The default setting for this register is 0.

10 1 **Green Clamp Select**
This bit determines whether the Green channel is clamped to ground or to midscale.

Table XXV. Green Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 37)

The default setting for this register is 0.

10 0 **Blue Clamp Select**
This bit determines whether the Blue channel is clamped to ground or to midscale.

Table XXVI. Blue Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 37)

The default setting for this register is 0.

11 **7–0 Sync Separator Threshold**
This register is used to set the responsiveness of the sync separator. It sets how many internal 5 MHz clock periods the sync separator must count to before toggling high or low. It works like a low-pass filter to ignore Hsync pulses in order to extract the Vsync signal. This register should be set to some number greater than the maximum Hsync pulsewidth. Note that the sync separator threshold uses an internal dedicated clock with a frequency of approximately 5 MHz.

The default for this register is 32.

12 **7–0 Pre-Coast**
This register allows the coast signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

0E 5 **Hsync Output Polarity**
This bit determines the polarity of the Hsync output and the SOG output. Table XI shows the effect of this option. SYNC indicates the logic state of the sync pulse.

Table XI. Hsync Output Polarity Settings

Setting	SYNC
0	Logic 1 (Positive Polarity)
1	Logic 0 (Negative Polarity)

The default setting for this register is 0.

0E 4 **Active Hsync Override**
This bit is used to override the automatic Hsync selection, To override, set this bit to Logic 1. When overriding, the active Hsync is set via Bit 3 in this register.

Table XII. Active Hsync Override Settings

Override	Result
0	Autodetermines the Active Interface
1	Override, Bit 3 Determines the Active Interface

The default for this register is 0.

0E 3 **Active Hsync Select**
This bit is used under two conditions. It is used to select the active Hsync when the override bit is set (Bit 4). Alternately, it is used to determine the active Hsync when not overriding but both Hsyncs are detected.

Table XIII. Active HSYNC Select Settings

Select	Result
0	HSYNC Input
1	Sync-on-Green Input

The default for this register is 0.

0E 2 **Vsync Output Invert**
This bit inverts the polarity of the Vsync output. Table XIV shows the effect of this option.

Table XIV. Vsync Output Invert Settings

Setting	Vsync Output
0	Invert
1	No Invert

The default setting for this register is 0.

0E 1 **Active Vsync Override**
This bit is used to override the automatic Vsync selection. To override, set this bit to Logic 1. When overriding, the active interface is set via Bit 0 in this register.

Table XV. Active Vsync Override Settings

Override	Result
0	Autodetermine the Active Vsync
1	Override, Bit 0 Determines the Active Vsync

The default for this register is 0.

0E 0 **Active Vsync Select**
This bit is used to select the active Vsync when the override bit is set (Bit 1).

Table XVI. Active Vsync Select Settings

Select	Result
0	Vsync Input
1	Sync Separator Output

The default for this register is 0.

0F 7 **Clamp Input Signal Source**
This bit determines the source of clamp timing.

Table XVII. Clamp Input Signal Source Settings

Clamp Function	Function
0	Internally Generated Clamp Signal
1	Externally Provided Clamp Signal

A 0 enables the clamp timing circuitry controlled by clamp placement and clamp duration. The clamp position and duration is counted from the leading edge of Hsync.

A 1 enables the external CLAMP input pin. The three channels are clamped when the CLAMP signal is active. The polarity of CLAMP is determined by the Clamp Polarity bit (Register 0FH, Bit 6).

The power-up default value is Clamp Function = 0.

0F 6 **Clamp Input Signal Polarity**
This bit determines the polarity of the externally provided CLAMP signal.

Table XVIII. Clamp Input Signal Polarity Settings

Clamp Function	Function
1	Active Low
0	Active High

A Logic 1 means that the circuit will clamp when CLAMP is low, and it will pass the signal to the ADC when CLAMP is high.

A Logic 0 means that the circuit will clamp when CLAMP is high, and it will pass the signal to the ADC when CLAMP is low.

The power-up default value is Clamp Polarity = 1.

0F 5 **Coast Select**
This bit is used to select the active Coast source. The choices are the Coast Input Pin or Vsync. If Vsync is selected the additional decision of using the Vsync input pin or the output from the sync separator needs to be made (Register 0E, Bits 1, 0).

Table XIX. Power-Down Settings

Select	Result
0	Coast Input Pin
1	Vsync (See above Text)

04 7–3 **Clock Phase Adjust**
A 5-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase.

The power-up default value is 16.

CLAMP TIMING

05 7–0 **Clamp Placement**
An 8-bit register that sets the position of the internally generated clamp.

When Clamp Function (Register 0FH, Bit 7) = 0, a clamp signal is generated internally, at a position established by the clamp placement and for a duration set by the clamp duration. Clamping is started (Clamp Placement) pixel periods after the trailing edge of Hsync. The clamp placement may be programmed to any value between 1 and 255.

The clamp should be placed during a time that the input signal presents a stable black-level reference, usually the back porch period between Hsync and the image.

When Clamp Function = 1, this register is ignored.

06 7–0 **Clamp Duration**
An 8-bit register that sets the duration of the internally generated clamp.

For the best results, the clamp duration should be set to include the majority of the black reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen, and a slow recovery from large changes in the average picture level (APL), or brightness.

When Clamp Function = 1, this register is ignored.

Hsync PULSEWIDTH

07 7–0 **Hsync Output Pulsewidth**
An 8-bit register that sets the duration of the Hsync output pulse.

The leading edge of the Hsync output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9883A then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of the Hsync output, which is also phase adjusted.

INPUT GAIN

08 7–0 **Red Channel Gain Adjust**
An 8-bit word that sets the gain of the Red channel. The AD9883A can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting REDGAIN to 255 corresponds to a 1.0 V input range. A REDGAIN of 0 establishes a 0.5 V input range. Note that increasing REDGAIN results in the picture having less contrast (the input signal uses fewer of the available converter codes). See Figure 2.

09 7–0 **Green Channel Gain Adjust**
An 8-bit word that sets the gain of the Green channel. See REDGAIN (08).

0A 7–0 **Blue Channel Gain Adjust**
An 8-bit word that sets the gain of the Blue channel. See REDGAIN (08).

INPUT OFFSET

0B 7–1 **Red Channel Offset Adjust**
A 7-bit offset binary word that sets the dc offset of the Red channel. One LSB of offset adjustment equals approximately one LSB change in the ADC offset. Therefore, the absolute magnitude of the offset adjustment scales as the gain of the channel is changed. A nominal setting of 63 results in the channel nominally clamping the back porch (during the clamping interval) to Code 00. An offset setting of 127 results in the channel clamping to Code 64 of the ADC. An offset setting of 0 clamps to Code –63 (off the bottom of the range). Increasing the value of Red Offset *decreases* the brightness of the channel.

0C 7–1 **Green Channel Offset Adjust**
A 7-bit offset binary word that sets the dc offset of the Green channel. See REDOFST (0B).

0D 7–1 **Blue Channel Offset Adjust**
A 7-bit offset binary word that sets the dc offset of the Green channel. See REDOFST (0B).

MODE CONTROL 1

0E 7 **Hsync Input Polarity Override**
This register is used to override the internal circuitry that determines the polarity of the Hsync signal going into the PLL.

Table IX. Hsync Input Polarity Override Settings

Override Bit	Function
0	Hsync Polarity Determined by Chip
1	Hsync Polarity Determined by User

The default for Hsync polarity override is 0 (polarity determined by chip).

0E 6 **HSPOL Hsync Input Polarity**
A bit that must be set to indicate the polarity of the Hsync signal that is applied to the PLL Hsync input.

Table X. Hsync Input Polarity Settings

HSPOL	Function
0	Active Low
1	Active High

Active Low means the leading edge of the Hsync pulse is negative going. All timing is based on the leading edge of Hsync, which is the falling edge. The rising edge has no effect.

Active high is inverted from the traditional Hsync, with a positive-going pulse. This means that timing will be based on the leading edge of Hsync, which is now the rising edge.

The device will operate if this bit is set incorrectly, but the internally generated clamp position, as established by Clamp Placement (Register 05H), will not be placed as expected, which may generate clamping errors.

The power-up default value is HSPOL = 1.

Table VI. Control Register Map (continued)

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
16H	R/W	7:0		Test Register	Reserved for future use.
17H	RO	7:0		Test Register	Reserved for future use.
18H	RO	7:0		Test Register	Reserved for future use.

*The AD9883A only updates the PLL divide ratio when the LSBs are written to (register 02H).

2-WIRE SERIAL CONTROL REGISTER DETAIL CHIP IDENTIFICATION

00 7–0 Chip Revision

An 8-bit register that represents the silicon revision. Revision 0 = 0000 0000, Revision 1 = 0000 0001, Revision 2 = 0000 0010.

PLL DIVIDER CONTROL

01 7–0 PLL Divide Ratio MSBs

The 8 most significant bits of the 12-bit PLL divide ratio PLLDIV. (The operational divide ratio is PLLDIV + 1.)

The PLL derives a master clock from an incoming Hsync signal. The master clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 2 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established some standard timing specifications that assist in determining the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (Table V).

However, many computer systems do not conform precisely to the recommendations, and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV will usually produce one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69H, PLLDIVL = DxH).

The AD9883A updates the full divide ratio only when the LSBs are changed. Writing to the MSB by itself will not trigger an update.

02 7–4 PLL Divide Ratio LSBs

The 4 least significant bits of the 12-bit PLL divide ratio PLLDIV. The operational divide ratio is PLLDIV + 1.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69H, PLLDIVL = DxH).

The AD9883A updates the full divide ratio only when this register is written to.

CLOCK GENERATOR CONTROL

03 7–6 VCO Range Select

Two bits that establish the operating range of the clock generator.

VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate).

The PLL gives the best jitter performance at high frequencies. For this reason, to output low pixel rates and still get good jitter performance, the PLL actually operates at a higher frequency but then divides down the clock rate afterwards. Table VII shows the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting.

Table VII. VCO Ranges

VCORNGE	Pixel Rate Range
00	12–32
01	32–64
10	64–110
11	110–140

The power-up default value is 01.

03 5–3 CURRENT Charge Pump Current

Three bits that establish the current driving the loop filter in the clock generator.

Table VIII. Charge Pump Currents

CURRENT	Current (μA)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

CURRENT must be set to correspond with the desired operating frequency (incoming pixel rate).

The power-up default value is current = 001.

Table VI. Control Register Map (continued)

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
0FH	R/W	7:1	0*******		Bit 7 – Clamp Function. Chooses between Hsync for Clamp signal or another external signal to be used for clamping. (Logic 0 = Hsync, Logic 1 = Clamp.)
			*1******		Bit 6 – Clamp Polarity. Valid only with external Clamp signal. (Logic 0 = Active High, Logic 1 Selects Active Low.)
			0***		Bit 5 – Coast Select. Logic 0 selects the coast input pins to be used for the PLL coast. Logic 1 selects Vsync to be used for the PLL coast.
			0*		Bit 4 – Coast Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 3 in register 0FH.)
			****1***		Bit 3 – Coast Polarity. Selects polarity of external Coast signal. (Logic 0 = Active Low, Logic 1 = Active High.)
			*****1**		Bit 2 – Seek Mode Override. (Logic 1 = Allow Low Power Mode, Logic 0 = Disallow Low Power Mode.)
			******1*		Bit 1 – PWRDN. Full Chip Power-Down, Active Low. (Logic 0 = Full Chip Power-Down, Logic 1 = Normal.)
10H	R/W	7:3	10111***	Sync-on-Green Threshold	Sync-on-Green Threshold. Sets the voltage level of the Sync-on-Green slicer's comparator.
			*****0**		Bit 2 – Red Clamp Select. Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37).
			******0*		Bit 1 – Green Clamp Select. Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37).
			*******0		Bit 0 – Blue Clamp Select. Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37).
11H	R/W	7:0	00100000	Sync Separator Threshold	Sync Separator Threshold. Sets how many internal 5 MHz clock periods the sync separator will count to before toggling high or low. This should be set to some number greater than the maximum Hsync or equalization pulsewidth.
12H	R/W	7:0	00000000	Pre-Coast	Pre-Coast. Sets the number of Hsync periods that Coast becomes active prior to Vsync.
13H	R/W	7:0	00000000	Post-Coast	Post-Coast. Sets the number of Hsync periods that Coast stays active following Vsync.
14H	RO	7:0		Sync Detect	Bit 7 – Hsync detect. It is set to Logic 1 if Hsync is present on the analog interface; otherwise it is set to Logic 0.
					Bit 6 – AHS: Active Hsync. This bit indicates which analog Hsync is being used. (Logic 0 = Hsync Input Pin, Logic 1 = Hsync from Sync-on-Green.)
					Bit 5 – Input Hsync Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.)
					Bit 4 – Vsync Detect. It is set to Logic 1 if Vsync is present on the analog interface; otherwise it is set to Logic 0.
					Bit 3 – AVS: Active Vsync. This bit indicates which analog Vsync is being used. (Logic 0 = Vsync Input Pin, Logic 1 = Vsync from Sync Separator.)
					Bit 2 – Output Vsync Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.)
					Bit 1 – Sync-on-Green Detect. It is set to Logic 1 if sync is present on the Green video input; otherwise it is set to 0.
					Bit 0 – Input Coast Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.)
15H	R/W	7:0	1111****	Test Register	Bits [7:4] Reserved for future use.
			****1***		Bit 3 – Must be set to 1 for proper operation.
			*****1**		Bit 2 – Must be set to 1 for proper operation.
			******1*		Bit 1 – 4:2:2 Output Formatting Mode (Logic 0 = 4:2:2 mode, Logic 1= 4:4:4 mode)
			*******1		Bit 0 – Must be set to 0 for proper operation.

2-Wire Serial Register Map

The AD9883A is initialized and controlled by a set of registers, which determine the operating modes. An external controller is employed to write and read the control registers through the two-line serial interface port.

Table VI. Control Register Map

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
00H	RO	7:0		Chip Revision	An 8-bit register that represents the silicon revision level. Revision 0 = 0000 0000.
01H*	R/W	7:0	01101001	PLL Div MSB	This register is for Bits [11:4] of the PLL divider. Greater values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed. This will give the PLL more time to lock.
02H*	R/W	7:4	1101****	PLL Div LSB	Bits [7:4] of this word are written to the LSBs [3:0] of the PLL divider word.
03H	R/W	7:3	01****** **001***		Bits [7:6] VCO Range. Selects VCO frequency range. (See PLL description.) Bits [5:3] Charge Pump Current. Varies the current that drives the low-pass filter. (See PLL description.)
04H	R/W	7:3	10000***	Phase Adjust	ADC Clock Phase Adjustment. Larger values mean more delay. (1 LSB = T/32)
05H	R/W	7:0	10000000	Clamp Placement	Places the Clamp signal an integer number of clock periods after the trailing edge of the Hsync signal.
06H	R/W	7:0	10000000	Clamp Duration	Number of clock periods that the Clamp signal is actively clamping.
07H	R/W	7:0	00100000	Hsync Output Pulsewidth	Sets the number of pixel clocks that HSOUT will remain active.
08H	R/W	7:0	10000000	Red Gain	Controls ADC input range (contrast) of each respective channel. Greater values give less contrast.
09H	R/W	7:0	10000000	Green Gain	
0AH	R/W	7:0	10000000	Blue Gain	
0BH	R/W	7:1	1000000*	Red Offset	Controls dc offset (brightness) of each respective channel. Greater values decrease brightness.
0CH	R/W	7:1	1000000*	Green Offset	
0DH	R/W	7:1	1000000*	Blue Offset	
0EH	R/W	7:0	0******* *1****** **0***** ***0**** ****0*** *****0** ******0* *******0	Sync Control	Bit 7 – Hsync Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 6 in register 0EH.) Bit 6 – Hsync Input Polarity. Indicates polarity of incoming Hsync signal to the PLL. (Logic 0 = Active Low, Logic 1 = Active High.) Bit 5 – Hsync Output Polarity. (Logic 0 = Logic High Sync, Logic 1 = Logic Low Sync.) Bit 4 – Active Hsync Override. If set to Logic 1, the user can select the Hsync to be used via Bit 3. If set to Logic 0, the active interface is selected via Bit 6 in register 14H. Bit 3 – Active Hsync Select. Logic 0 selects Hsync as the active sync. Logic 1 selects Sync-on-Green as the active sync. Note that the indicated Hsync will be used only if Bit 4 is set to Logic 1 or if both syncs are active. (Bits 1, 7 = Logic 1 in register 14H.) Bit 2 – Vsync Output Invert. (Logic 1 = No Invert, Logic 0 = Invert.) Bit 1 – Active Vsync Override. If set to Logic 1, the user can select the Vsync to be used via Bit 0. If set to Logic 0, the active interface is selected via Bit 3 in register 14H. Bit 0 – Active Vsync Select. Logic 0 selects Raw Vsync as the output Vsync. Logic 1 selects Sync Separated Vsync as the output Vsync. Note that the indicated Vsync will be used only if Bit 1 is set to Logic 1.

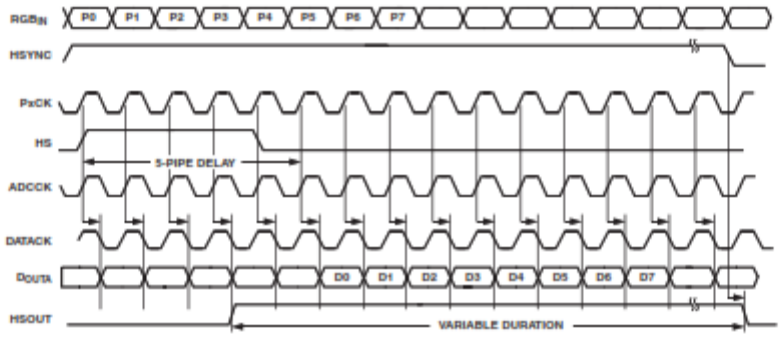


Figure 8. 4:4:4 Mode (For RGB and YUV)

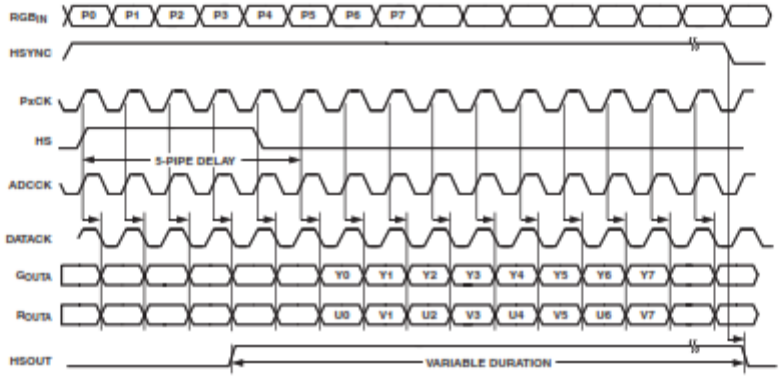


Figure 9. 4:2:2 Mode (For YUV Only)

Table V. Recommended VCO Range and Charge Pump Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate	Horizontal Frequency	Pixel Rate	AD9883AKST		AD9883ABST	
					VCORNGE	Current	VCORNGE	Current
VGA	640 × 480	60 Hz	31.5 kHz	25.175 MHz	00	110	00	011
		72 Hz	37.7 kHz	31.500 MHz	00	110	01	010
		75 Hz	37.5 kHz	31.500 MHz	00	110	01	010
		85 Hz	43.3 kHz	36.000 MHz	01	100	01	010
SVGA	800 × 600	56 Hz	35.1 kHz	36.000 MHz	01	100	01	010
		60 Hz	37.9 kHz	40.000 MHz	01	100	01	011
		72 Hz	48.1 kHz	50.000 MHz	01	101	01	100
		75 Hz	46.9 kHz	49.500 MHz	01	101	01	100
		85 Hz	53.7 kHz	56.250 MHz	01	101	01	101
XGA	1024 × 768	60 Hz	48.4 kHz	65.000 MHz	10	101	10	011
		70 Hz	56.5 kHz	75.000 MHz	10	100	10	011
		75 Hz	60.0 kHz	78.750 MHz	10	100	10	011
		80 Hz	64.0 kHz	85.500 MHz	10	101	10	100
		85 Hz	68.3 kHz	94.500 MHz	10	101	10	100
SXGA	1280 × 1024	60 Hz	64.0 kHz	108.000 MHz	10	110	10	101
		75 Hz	80.0 kHz	135.000 MHz	11	110	11	101

Timing

The following timing diagrams show the operation of the AD9883A.

The output data clock signal is created so that its rising edge always occurs between data transitions, and can be used to latch the output data externally.

There is a pipeline in the AD9883A, which must be flushed before valid data becomes available. This means four data sets are presented before valid data is available.

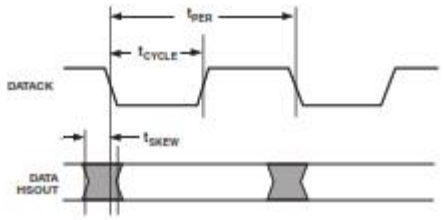


Figure 7. Output Timing

Hsync Timing

Horizontal Sync (Hsync) is processed in the AD9883A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted, with respect to Hsync, through a full 360° in 32 steps via the Phase Adjust Register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOUT) and data clock (DATACK).

Three things happen to Horizontal Sync in the AD9883A. First, the polarity of Hsync input is determined and will thus have a known output polarity. The known output polarity can be programmed either active high or active low (register 0EH, Bit 5). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via register 07H. HSOUT is the sync signal that should be used to drive the rest of the display system.

Coast Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the COAST input and function are unnecessary, and should not be used and the pin should be permanently connected to the inactive state.

In some systems, however, Hsync is disturbed during the Vertical Sync period (Vsync). In some cases, Hsync pulses disappear. In other systems, such as those that employ Composite Sync (Csync) signals or embedded Sync-on-Green (SOG), Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it will attempt to lock to this new frequency, and will have changed frequency by the end of the Vsync period. It will then take a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a "tearing" of the image at the top of the display.

The COAST input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and allows the clock to free-run at its then-current frequency. The PLL can free-run for several lines without significant frequency drift.

The PLL characteristics are determined by the loop filter design, by the PLL Charge Pump Current, and by the VCO range setting. The loop filter design is illustrated in Figure 6. Recommended settings of VCO range and charge pump current for VESA standard display modes are listed in Table V.

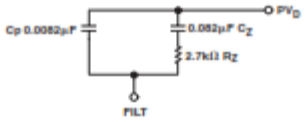


Figure 6. PLL Loop Filter Detail

Four programmable registers are provided to optimize the performance of the PLL. These registers are:

1. The 12-Bit Divisor Register. The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 12 MHz to 110 MHz. The Divisor Register controls the exact multiplication factor. This register may be set to any value between 221 and 4095. (The divide ratio that is actually used is the programmed divide ratio plus one.)
2. The 2-Bit VCO Range Register. To improve the noise performance of the AD9883A, the VCO operating frequency range is divided into three overlapping regions. The VCO Range Register sets this operating range. The frequency ranges for the lowest and highest regions are shown in Table II.

Table II. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz) AD9883AKST	AD9883ABST
0	0	12–32	12–30
0	1	32–64	30–60
1	0	64–110	60–120
1	1	110–140	120–140

3. The 3-Bit Charge Pump Current Register. This register allows the current that drives the low-pass loop filter to be varied. The possible current values are listed in Table III.

Table III. Charge Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

4. The 5-Bit Phase Adjust Register. The phase of the generated sampling clock may be shifted to locate an optimum sampling point within a clock cycle. The Phase Adjust Register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin.

   The COAST pin is used to allow the PLL to continue to run at the same frequency, in the absence of the incoming Hsync signal or during disturbances in Hsync (such as equalization pulses). This may be used during the vertical sync period, or any other time that the Hsync signal is unavailable. The polarity of the COAST signal may be set through the Coast Polarity Register. Also, the polarity of the Hsync signal may be set through the Hsync Polarity Register. If not using automatic polarity detection, the Hsync and COAST Polarity bits should be set to match the respective polarities of the input signals.

Power Management

The AD9883A uses the activity detect circuits, the active interface bits in the serial bus, the active interface override bits, and the power-down bit to determine the correct power state. There are three power states, full-power, seek mode, and power-down. Table IV summarizes how the AD9883A determines what power mode to be in and which circuitry is powered on/off in each of these modes. The power-down command has priority over the automatic circuitry.

Table IV. Power-Down Mode Descriptions

Mode	Inputs Power-Down[1]	Sync Detect[2]	Powered On or Comments
Full-Power	1	1	Everything
Seek Mode	1	0	Serial Bus, Sync Activity Detect, SOG, Band Gap Reference
Power-Down	0	X	Serial Bus, Sync Activity Detect, SOG, Band Gap Reference

NOTES
[1]Power-down is controlled via Bit 1 in serial bus register 0FH.
[2]Sync detect is determined by OR-ing Bits 7, 4, and 1 in serial bus register 14H.

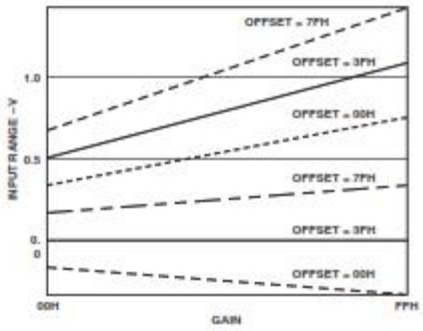


Figure 2. Gain and Offset Control

Gain and Offset Control

The AD9883A can accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (Red Gain, Green Gain, and Blue Gain). Note that *increasing* the gain setting results in an image with *less* contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 7-bit registers (Red Offset, Green Offset, Blue Offset) provide independent settings for each channel. The offset controls provide a ±63 LSB adjustment range. This range is connected with the full-scale range, so if the input range is doubled (from 0.5 V to 1.0 V) then the offset step size is also doubled (from 2 mV per step to 4 mV per step).

Figure 2 illustrates the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, so changing the full-scale range also changes the offset. The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale *range* is not affected, but the full-scale *level* is shifted by the same amount as the zero scale level.

Sync-on-Green

The Sync-on-Green input operates in two steps. First, it sets a baseline clamp level off of the incoming video signal with a negative peak detector. Second, it sets the sync trigger level to a programmable level (typically 150 mV) above the negative peak. The Sync-on-Green input must be ac-coupled to the Green analog input through its own capacitor, as shown in Figure 3. The value of the capacitor must be 1 nF ± 20%. If Sync-on-Green is not used, this connection is not required. Note that the Sync-on-Green signal is always negative polarity.

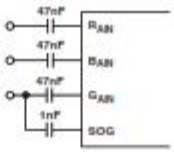


Figure 3. Typical Clamp Configuration

Clock Generation

A phase locked loop (PLL) is employed to generate the pixel clock. In this PLL, the Hsync input provides a reference frequency. A voltage controlled oscillator (VCO) generates a much higher pixel clock frequency. This pixel clock is divided by the PLL divide value (registers 01H and 02H) and phase compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period during which the signal is slewing from the old pixel amplitude and settling at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (Figure 4). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter, and the stable pixel time becomes shorter as well.

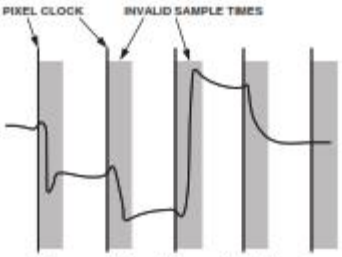


Figure 4. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined, and must also be subtracted from the stable pixel time.

Considerable care has been taken in the design of the AD9883A's clock generation circuit to minimize jitter. As indicated in Figure 5, the clock jitter of the AD9883A is less than 5% of the total pixel time in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

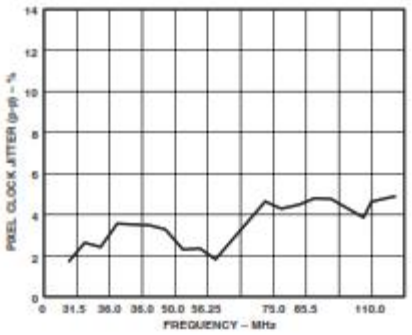


Figure 5. Pixel Clock Jitter vs. Frequency

At that point the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9883A inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The ultrawide bandwidth inputs of the AD9883A (300 MHz) can track the input signal continuously as it moves from one pixel level to the next, and digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. It has been shown that a small inductor in series with the input is effective in rolling off the input bandwidth slightly and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0 High Speed Signal Chip Bead inductor in the circuit of Figure 1 gives good results in most applications.

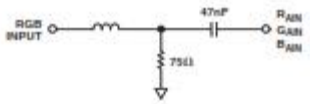


Figure 1. Analog Input Interface Circuit

Hsync, Vsync Inputs

The interface also takes a horizontal sync signal, which is used to generate the pixel clock and clamp timing. This can be either a sync signal directly from the graphics source, or a preprocessed TTL or CMOS level signal.

The Hsync input includes a Schmitt trigger buffer for immunity to noise and signals with long rise times. In typical PC based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required.

Serial Control Port

The serial control port is designed for 3.3 V logic. If there are 5 V drivers on the bus, these pins should be protected with 150 Ω series resistors placed between the pull-up resistors and the input pins.

Output Signal Handling

The digital outputs are designed and specified to operate from a 3.3 V power supply (V_{DD}). They can also work with a V_{DD} as low as 2.5 V for compatibility with other 2.5 V logic.

Clamping

RGB Clamping

To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board A/D converters.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground and black is at 300 mV. Then white is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which must be removed for proper capture by the AD9883A.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced which results in the A/D converters producing a black output (code 00h) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most PC graphics systems, black is transmitted between active video lines. With CRT displays, when the electron beam has completed writing a horizontal line on the screen (at the right side), the beam is deflected quickly to the left side of the screen (called horizontal retrace) and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is virtually always a period following Hsync, called the back porch, where a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time (with External Clamp = 1). The polarity of this signal is set by the Clamp Polarity bit.

A simpler method of clamp timing employs the AD9883A internal clamp timing generator. The Clamp Placement register is programmed with the number of pixel times that should pass after the trailing edge of HSYNC before clamping starts. A second register (Clamp Duration) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync because, though Hsync duration can vary widely, the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 09H (providing 9 pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 14H (giving the clamp 20 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there will be a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it will take excessively long for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovering from a step error of 100 mV to within 1/2 LSB in 10 lines with a clamp duration of 20 pixel periods on a 60 Hz SXGA signal.

YUV Clamping

YUV graphic signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) can be at the midpoint of the graphics signal rather than at the bottom. For these signals, it can be necessary to clamp to the midscale range of the A/D converter range (80H) rather than at the bottom of the A/D converter range (00H).

Clamping to midscale rather than to ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that they can be clamped to either midscale or ground independently. These bits are located in register 10H and are Bits 0–2. The midscale reference voltage that each A/D converter clamps to is provided on the MIDSCV pin, (Pin 37). This pin should be bypassed to ground with a 0.1 μF capacitor, (even if midscale clamping is not required).

PIN FUNCTION DESCRIPTIONS (continued)

Pin Name	Function
CLAMP	External Clamp Input This logic input may be used to define the time during which the input signal is clamped to ground. It should be exercised when the reference dc level is known to be present on the analog input channels, typically during the back porch of the graphics signal. The CLAMP pin is enabled by setting control bit Clamp Function to 1, (register 0FH, Bit 7, default is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the Hsync input. The logic sense of this pin is controlled by Clamp Polarity register 0FH, Bit 6. When not used, this pin must be grounded and Clamp Function programmed to 0.
COAST	Clock Generator Coast Input (Optional) This input may be used to cause the pixel clock generator to stop synchronizing with Hsync and continue producing a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync pulses during the vertical interval. The COAST signal is generally *not* required for PC-generated signals. The logic sense of this pin is controlled by Coast Polarity (register 0FH, Bit 3). When not used, this pin may be grounded and Coast Polarity programmed to 1, or tied HIGH (to V_D through a 10 kΩ resistor) and Coast Polarity programmed to 0. Coast Polarity defaults to 1 at power-up.
REF BYPASS	Internal Reference BYPASS Bypass for the internal 1.25 V band gap reference. It should be connected to ground through a 0.1 µF capacitor. The absolute accuracy of this reference is ±4%, and the temperature coefficient is ±50 ppm, which is adequate for most AD9883A applications. If higher accuracy is required, an external reference may be employed instead.
MIDSCV	Midscale Voltage Reference BYPASS Bypass for the internal midscale voltage reference. It should be connected to ground through a 0.1 µF capacitor. The exact voltage varies with the gain setting of the Blue channel.
FILT	External Filter Connection For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node.
POWER SUPPLY	
V_D	Main Power Supply These pins supply power to the main elements of the circuit. They should be filtered and as quiet as possible.
V_{DD}	Digital Output Power Supply A large number of output pins (up to 25) switching at high speed (up to 110 MHz) generates a lot of power supply transients (noise). These supply pins are identified separately from the V_D pins so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9883A is interfacing with lower voltage logic, V_{DD} may be connected to a lower supply voltage (as low as 2.5 V) for compatibility.
PV_D	Clock Generator Power Supply The most sensitive portion of the AD9883A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide quiet, noise-free power to these pins.
GND	Ground The ground return for all circuitry on-chip. It is recommended that the AD9883A be assembled on a single solid ground plane, with careful attention given to ground current paths.

DESIGN GUIDE

General Description

The AD9883A is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The circuit is ideal for providing a computer interface for HDTV monitors or as the front end to high performance video scan converters. Implemented in a high performance CMOS process, the interface can capture signals with pixel rates up to 110 MHz.

The AD9883A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of only 500 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

Digital Inputs

All digital inputs on the AD9883A operate to 3.3 V CMOS levels. However, all digital inputs are 5 V tolerant. Applying 5 V to them will not cause any damage.

Input Signal Handling

The AD9883A has three high impedance analog input pins for the Red, Green, and Blue channels. They will accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-pin D connector, or via BNC connectors. The AD9883A should be located as close as practical to the input connector. Signals should be routed via matched-impedance traces (normally 75 Ω) to the IC input pins.

PIN FUNCTION DESCRIPTIONS

Pin Name	Function
OUTPUTS	
HSOUT	Horizontal Sync Output A reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATACK and Data, data timing with respect to horizontal sync can always be determined.
VSOUT	Vertical Sync Output A reconstructed and phase-aligned version of the video Vsync. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes is set by the graphics transmitter.
SOGOUT	Sync-On-Green Slicer Output This pin outputs either the signal from the Sync-on-Green slicer comparator or an unprocessed but delayed version of the Hsync input. See the Sync Processing Block Diagram (Figure 12) to view how this pin is connected. (Note: Besides slicing off SOG, the output from this pin gets no other additional processing on the AD9883A. Vsync separation is performed via the sync separator.)
SERIAL PORT (2-Wire)	
SDA	Serial Port Data I/O
SCL	Serial Port Data Clock
A0	Serial Port Address Input 1 For a full description of the 2-wire serial register and how it works, refer to the 2-Wire Serial Control Port section.
DATA OUTPUTS	
RED	Data Output, Red Channel
GREEN	Data Output, Green Channel
BLUE	Data Output, Blue Channel The main data outputs. Bit 7 is the MSB. The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained. For exact timing information, refer to Figures 7, 8, and 9.
DATA CLOCK OUTPUT	
DATACK	Data Output Clock This is the main clock output signal used to strobe the output data and HSOUT into external logic. It is produced by the internal clock generator and is synchronous with the internal pixel sampling clock. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATACK, and HSOUT outputs are all moved, so the timing relationship among the signals is maintained.
INPUTS	
R_{AIN}	Analog Input for Red Channel
G_{AIN}	Analog Input for Green Channel
B_{AIN}	Analog Input for Blue Channel High impedance inputs that accept the Red, Green, and Blue channel graphics signals, respectively. (The three channels are identical, and can be used for any colors, but colors are assigned for convenient reference.) They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.
HSYNC	Horizontal Sync Input This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin is controlled by serial register 0EH Bit 6 (Hsync Polarity). Only the leading edge of Hsync is active; the trailing edge is ignored. When Hsync Polarity = 0, the falling edge of Hsync is used. When Hsync Polarity = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5 V.
VSYNC	Vertical Sync Input This is the input for vertical sync.
SOGIN	Sync-on-Green Input This input is provided to assist with processing signals with embedded sync, typically on the Green channel. The pin is connected to a high speed comparator with an internally generated threshold. The threshold level can be programmed in 10 mV steps to any voltage between 10 mV and 330 mV above the negative peak of the input signal. The default voltage threshold is 150 mV. When connected to an ac-coupled graphics signal with embedded sync, it will produce a noninverting digital output on SOGOUT. (This is usually a composite sync signal, containing both vertical and horizontal sync information that must be separated before passing the horizontal sync signal to Hsync.) When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green section.

PIN CONFIGURATION

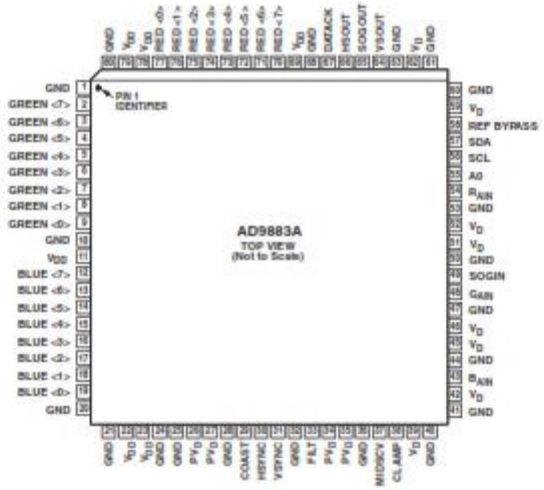


Table I. Complete Pinout List

Pin Type	Mnemonic	Function	Value	Pin No.
Inputs	R_{AIN}	Analog Input for Converter R	0.0 V to 1.0 V	54
	G_{AIN}	Analog Input for Converter G	0.0 V to 1.0 V	48
	B_{AIN}	Analog Input for Converter B	0.0 V to 1.0 V	43
	HSYNC	Horizontal SYNC Input	3.3 V CMOS	30
	VSYNC	Vertical SYNC Input	3.3 V CMOS	31
	SOGIN	Input for Sync-on-Green	0.0 V to 1.0 V	49
	CLAMP	Clamp Input (External CLAMP Signal)	3.3 V CMOS	38
	COAST	PLL COAST Signal Input	3.3 V CMOS	29
Outputs	Red [7:0]	Outputs of Converter Red, Bit 7 is the MSB	3.3 V CMOS	70–77
	Green [7:0]	Outputs of Converter Green, Bit 7 is the MSB	3.3 V CMOS	2–9
	Blue [7:0]	Outputs of Converter Blue, Bit 7 is the MSB	3.3 V CMOS	12–19
	DATACK	Data Output Clock	3.3 V CMOS	67
	HSOUT	HSYNC Output (Phase-Aligned with DATACK)	3.3 V CMOS	66
	VSOUT	VSYNC Output (Phase-Aligned with DATACK)	3.3 V CMOS	64
	SOGOUT	Sync-on-Green Slicer Output	3.3 V CMOS	65
References	REF BYPASS	Internal Reference Bypass	1.25 V	58
	MIDSCV	Internal Midscale Voltage Bypass		37
	FILT	Connection for External Filter Components for Internal PLL		33
Power Supply	V_D	Analog Power Supply	3.3 V	39, 42, 45, 46, 51, 52, 59, 62
	V_{DD}	Output Power Supply	3.3 V	11, 22, 23, 69, 78, 79
	PV_D	PLL Power Supply	3.3 V	26, 27, 34, 35
	GND	Ground	0 V	1, 10, 20, 21, 24, 25, 28, 32, 36, 40, 41, 44, 47, 50, 53, 60, 61, 63, 68, 80
Control	SDA	Serial Port Data I/O	3.3 V CMOS	57
	SCL	Serial Port Data Clock (100 kHz Maximum)	3.3 V CMOS	56
	A0	Serial Port Address Input 1	3.3 V CMOS	55

ABSOLUTE MAXIMUM RATINGS*

V_D	3.6 V
V_{DD}	3.6 V
Analog Inputs	V_D to 0.0 V
VREF IN	V_D to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.
II. 100% production tested at 25°C and sample tested at specified temperatures.
III. Sample tested only.
IV. Parameter is guaranteed by design and characterization testing.
V. Parameter is a typical value only.
VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9883AKST-140	0°C to 70°C	LQFP	ST-80
AD9883AKST-110	0°C to 70°C	LQFP	ST-80
AD9883AKSTZ-110*	0°C to 70°C	LQFP	ST-80
AD9883AKSTZ-140*	0°C to 70°C	LQFP	ST-80
AD9883ABST-110	–40°C to +85°C	LQFP	ST-80
AD9883ABST-140	–40°C to +85°C	LQFP	ST-80
AD9883ABST-RL110	–40°C to +85°C	LQFP	ST-80
AD9883ABST-RL140	–40°C to +85°C	LQFP	ST-80
AD9883A/PCB	25°C	Evaluation Board	

*Lead-free product

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9883A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Parameter	Temp	Test Level	AD9883ABST–110 Min	AD9883ABST–110 Typ	AD9883ABST–110 Max	AD9883ABST–140 Min	AD9883ABST–140 Typ	AD9883ABST–140 Max	Unit
POWER SUPPLY									
V_D Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.6	2.2	3.3	3.6	V
P_{VD} Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
I_D Supply Current (V_D)	25°C	V		132			163		mA
I_{DD} Supply Current (V_{DD})[2]	25°C	V		19			24		mA
IP_{VD} Supply Current (P_{VD})	25°C	V		8			10		mA
Total Power Dissipation	Full	VI		525	700		650	850	mW
Power-Down Supply Current	Full	VI		5	15		5	15	mA
Power-Down Dissipation	Full	VI		16.5	33		16.5	33	mW
DYNAMIC PERFORMANCE									
Analog Bandwidth, Full Power	25°C	V		300			300		MHz
Transient Response	25°C	V		2			2		ns
Overvoltage Recovery Time	25°C	V		1.5			1.5		ns
Signal-to-Noise Ratio (SNR)	25°C	V		44			43		dB
(Without Harmonics)	Full	V		43			42		dB
f_{IN} = 40.7 MHz									
Crosstalk	Full	V		55			55		dBc
THERMAL CHARACTERISTICS									
θ_{JC} Junction-to-Case Thermal Resistance	V			16			16		°C/W
θ_{JA} Junction-to-Ambient Thermal Resistance	V			35			35		°C/W

NOTES
[1]VCO Range = 10, Charge Pump Current = 110, PLL Divider = 1693.
[2]DATACK Load = 15 pF, Data Load = 5 pF.

Specifications subject to change without notice.

Analog Interface (V_R = 3.3 V, V_{DD} = 3.3 V, ADC Clock = Maximum Conversion Rate, unless otherwise noted.)

Parameter	Temp	Test Level	AD9883ABST-110 Min	AD9883ABST-110 Typ	AD9883ABST-110 Max	AD9883ABST-140 Min	AD9883ABST-140 Typ	AD9883ABST-140 Max	Unit
RESOLUTION				8			8		Bits
DC ACCURACY									
Differential Nonlinearity	25°C	I		±0.5	+1.25/–1.0		±0.5	+1.5/–1.0	LSB
	Full	VI			+1.5/–1.0			+1.81/–1.0	LSB
Integral Nonlinearity	25°C	I		±0.5	±1.85		±0.5	±1.85	LSB
	Full	VI			±3.2			±3.2	LSB
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			V p-p
Gain Tempco	25°C	V		100			100		ppm/°C
Input Bias Current	25°C	IV			1			1	µA
	Full	IV			2			2	µA
Input Offset Voltage	Full	VI		7	75		7	75	mV
Input Full-Scale Matching	Full	VI		1.5	8.0		1.5	10.0	% FS
Offset Adjustment Range	Full	VI	46	49	52	46	49	52	% FS
REFERENCE OUTPUT									
Output Voltage	Full	VI	1.19	1.25	1.33	1.19	1.25	1.33	V
Temperature Coefficient	Full	V		±100			±100		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	110			140			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Data to Clock Skew	Full	IV	–0.5		+2.0	–0.5		+2.0	ns
t_{BUFF}	Full	VI	4.7			4.7			µs
t_{STAH}	Full	VI	4.0			4.0			µs
t_{DHO}	Full	VI	0			0			µs
t_{DAL}	Full	VI	4.7			4.7			µs
t_{DAH}	Full	VI	4.0			4.0			µs
t_{DSU}	Full	VI	250			250			µs
t_{STASU}	Full	VI	4.7			4.7			µs
t_{STOSU}	Full	VI	4.0			4.0			µs
HSYNC Input Frequency	Full	IV	15		110	15		110	kHz
Maximum PLL Clock Rate	Full	VI	110			140			MHz
Minimum PLL Clock Rate	Full	IV			12			12	MHz
PLL Jitter	25°C	IV		400	700[1]		400	700[1]	ps p-p
	Full	IV			1100[1]			1100[1]	ps p-p
Sampling Phase Tempco	Full	IV		15			15		ps/°C
DIGITAL INPUTS									
Input Voltage, High (V_{IH})	Full	VI	2.5			2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8	V
Input Current, High (I_{IH})	Full	V			–1.0			–1.0	µA
Input Current, Low (I_{IL})	Full	V			1.0			1.0	µA
Input Capacitance	+25°C	V		3			3		pF
DIGITAL OUTPUTS									
Output Voltage, High (V_{OH})	Full	VI	V_D – 0.1			V_D – 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.1			0.1	V
Duty Cycle, DATACK	Full	IV	45	50	55	45	50	55	%
Output Coding				Binary			Binary		

Parameter	Temp	Test Level	AD9883AKST-110 Min	AD9883AKST-110 Typ	AD9883AKST-110 Max	AD9883AKST-140 Min	AD9883AKST-140 Typ	AD9883AKST-140 Max	Unit
DIGITAL OUTPUTS									
Output Voltage, High (V_{OH})	Full	VI	V_D – 0.1			V_D – 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.1			0.1	V
Duty Cycle DATACK	Full	IV	45	50	55	45	50	55	%
Output Coding				Binary			Binary		
POWER SUPPLY									
V_D Supply Voltage	Full	IV	3.0	3.3	3.6	3.15	3.3	3.6	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.6	2.2	3.3	3.6	V
P_{VD} Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
I_D Supply Current (V_D)	25°C	V		132			180		mA
I_{DD} Supply Current (V_{DD})[2]	25°C	V		19			26		mA
IP_{VD} Supply Current (P_{VD})	25°C	V		8			11		mA
Total Power Dissipation	Full	VI		525	650		650	800	mW
Power-Down Supply Current	Full	VI		5	10		5	10	mA
Power-Down Dissipation	Full	VI		16.5	33		16.5	33	mW
DYNAMIC PERFORMANCE									
Analog Bandwidth, Full Power	25°C	V		300			300		MHz
Transient Response	25°C	V		2			2		ns
Overvoltage Recovery Time	25°C	V		1.5			1.5		ns
Signal-to-Noise Ratio (SNR)	25°C	V		44			43		dB
(Without Harmonics)	Full	V		43			42		dB
f_{IN} = 40.7 MHz									
Crosstalk	Full	V		55			55		dBc
THERMAL CHARACTERISTICS									
θ_{JC} Junction-to-Case Thermal Resistance		V		16			16		°C/W
θ_{JA} Junction-to-Ambient Thermal Resistance		V		35			35		°C/W

NOTES
[1]VCO Range = 10, Charge Pump Current = 110, PLL Divider = 1693.
[2]DATACK Load = 15 pF, Data Load = 5 pF.

Specifications subject to change without notice.

AD9883A–SPECIFICATIONS

Analog Interface (V_D = 3.3 V, V_{DD} = 3.3 V, ADC Clock = Maximum Conversion Rate, unless otherwise noted.)

Parameter	Temp	Test Level	AD9883AKST-110 Min	AD9883AKST-110 Typ	AD9883AKST-110 Max	AD9883AKST-140 Min	AD9883AKST-140 Typ	AD9883AKST-140 Max	Unit
RESOLUTION				8			8		Bits
DC ACCURACY									
Differential Nonlinearity	25°C	I		±0.5	+1.25/–1.0		±0.5	+1.35/–1.0	LSB
	Full	VI			+1.35/–1.0			+1.45/–1.0	LSB
Integral Nonlinearity	25°C	I		±0.5	±1.85		±0.5	±2.0	LSB
	Full	VI			±2.0			±2.3	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			V p-p
Gain Tempco	25°C	V		100			100		ppm/°C
Input Bias Current	25°C	IV			1			1	µA
	Full	IV			1			1	µA
Input Offset Voltage	Full	VI		7	50		7	70	mV
Input Full-Scale Matching	Full	VI		1.5	6.0		1.5	8.0	% FS
Offset Adjustment Range	Full	VI	46	49	52	46	49	52	% FS
REFERENCE OUTPUT									
Output Voltage	Full	VI	1.20	1.25	1.32	1.20	1.25	1.32	V
Temperature Coefficient	Full	V		±50			±50		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	110			140			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Data to Clock Skew	Full	IV	–0.5		+2.0	–0.5		+2.0	ns
t_{BUFF}	Full	VI	4.7			4.7			µs
t_{STAH}	Full	VI	4.0			4.0			µs
t_{DHO}	Full	VI	0			0			µs
t_{DAL}	Full	VI	4.7			4.7			µs
t_{DAH}	Full	VI	4.0			4.0			µs
t_{DSU}	Full	VI	250			250			ns
t_{STASU}	Full	VI	4.7			4.7			µs
t_{STOSU}	Full	VI	4.0			4.0			µs
HSYNC Input Frequency	Full	IV	15		110	15		110	kHz
Maximum PLL Clock Rate	Full	VI	110			140			MHz
Minimum PLL Clock Rate	Full	IV			12			12	MHz
PLL Jitter	25°C	IV		400	700[1]		400	700[1]	ps p-p
	Full	IV			1000[1]			1000[1]	ps p-p
Sampling Phase Tempco	Full	IV		15			15		ps/°C
DIGITAL INPUTS									
Input Voltage, High (V_{IH})	Full	VI	2.5			2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8	V
Input Voltage, High (V_{IH})	Full	V			–1.0			–1.0	µA
Input Voltage, Low (V_{IL})	Full	V			+1.0			+1.0	µA
Input Capacitance	25°C	V		3			3		pF

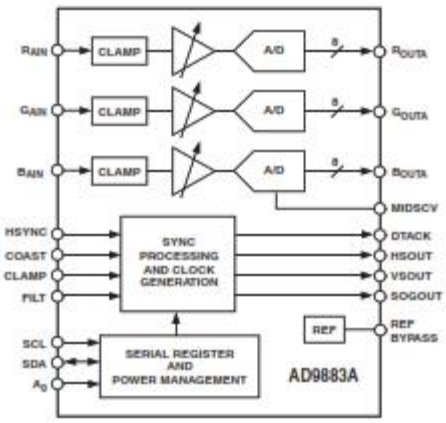
110 MSPS/140 MSPS Analog Interface for Flat Panel Displays

AD9883A

FEATURES
- Industrial Temperature Range Operation
- 140 MSPS Maximum Conversion Rate
- 300 MHz Analog Bandwidth
- 0.5 V to 1.0 V Analog Input Range
- 500 ps p-p PLL Clock Jitter at 110 MSPS
- 3.3 V Power Supply
- Full Sync Processing
- Sync Detect for Hot Plugging
- Midscale Clamping
- Power-Down Mode
- Low Power: 500 mW Typical
- 4:2:2 Output Format Mode

APPLICATIONS
- RGB Graphics Processing
- LCD Monitors and Projectors
- Plasma Display Panels
- Scan Converters
- Microdisplays
- Digital TV

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9883A is a complete 8-bit, 140 MSPS, monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 × 1024 at 75 Hz).

The AD9883A includes a 140 MHz triple ADC with internal 1.25 V reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and Hsync and COAST signals. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9883A's on-chip PLL generates a pixel clock from the Hsync input. Pixel clock output frequencies range from 12 MHz to 140 MHz. PLL clock jitter is 500 ps p-p typical at 140 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of Hsync. A sampling phase adjustment is provided. Data, Hsync, and clock output phase relationships are maintained. The AD9883A also offers full sync processing for composite sync and sync-on-green applications.

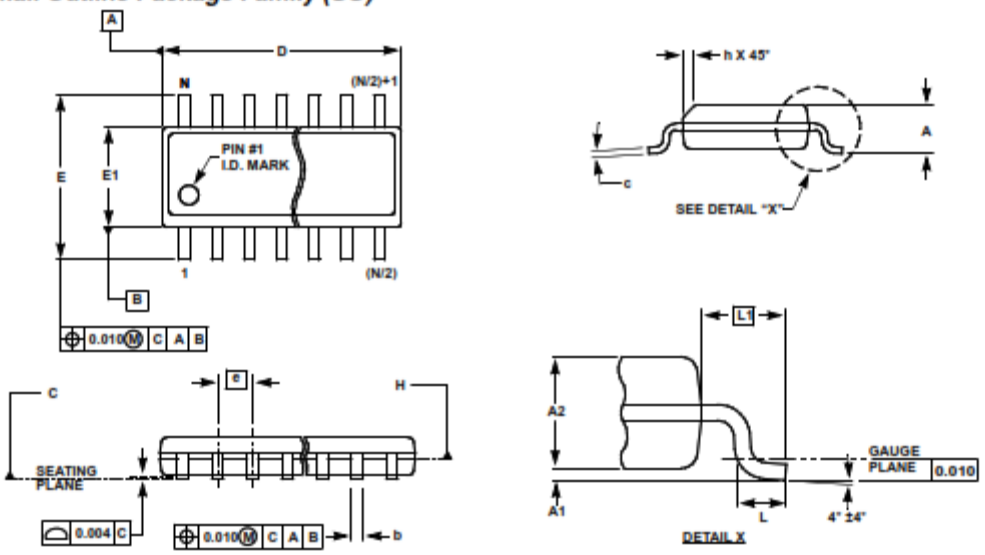
A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a 2-wire serial interface.

Fabricated in an advanced CMOS process, the AD9883A is provided in a space-saving 80-lead LQFP surface-mount plastic package and is specified over the –40°C to +85°C temperature range.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

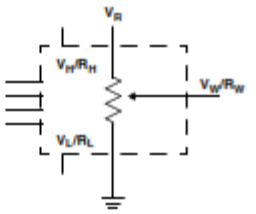
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

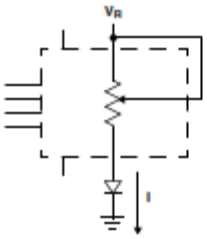
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Basic Configurations of Electronic Potentiometers

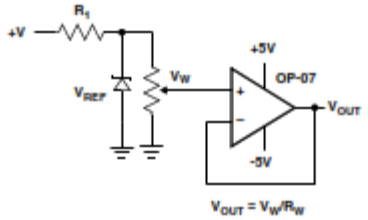


THREE TERMINAL POTENTIOMETER;
VARIABLE VOLTAGE DIVIDER

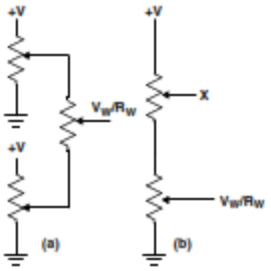


TWO TERMINAL VARIABLE RESISTOR;
VARIABLE CURRENT

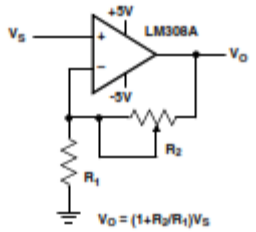
Basic Circuits



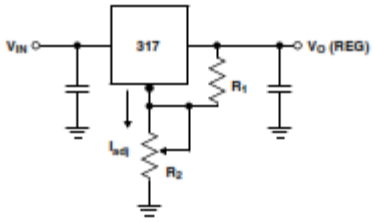
BUFFERED REFERENCE VOLTAGE



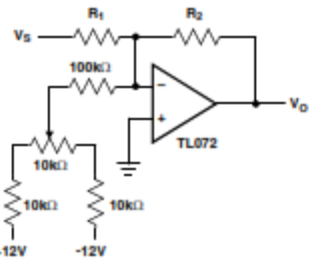
CASCADING TECHNIQUES



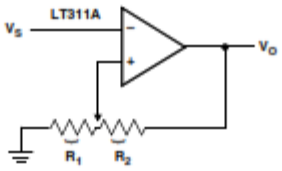
NONINVERTING AMPLIFIER



VOLTAGE REGULATOR



OFFSET VOLTAGE ADJUSTMENT



(FOR ADDITIONAL CIRCUITS SEE AN1145)

COMPARATOR WITH HYSTERESIS

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW, the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a 7-bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The value of the counter is stored in non-volatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9Cxxx, move the wiper and deselect the device without having to store the latest wiper position in non-volatile memory. After the wiper movement is performed as previously described and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-down/up cycle recalled the previously stored data.

This procedure allows the system to always power-up to a pre-set value stored in non-volatile memory; then during system operation, minor adjustments could be made. The adjustments might be based on user preference, i.e.: system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↘	H	Wiper Up
L	↘	L	Wiper Down
↗	H	X	Store Wiper Position
H	X	X	Standby Current
↗	L	X	No Store, Return to Standby
↘	L	H	Wiper Up (not recommended)
↘	L	L	Wiper Down (not recommended)

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Performance Characteristics

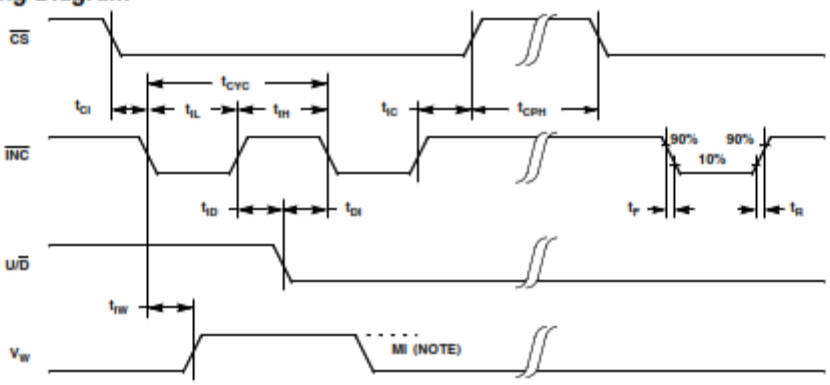
Contact the factory for more information.

Applications Information

Electronic digitally controlled (XCDP) potentiometers provide three powerful application advantages:

1. The variability and reliability of a solid-state potentiometer.
2. The flexibility of computer-based digital controls.
3. The retentivity of non-volatile memory used for the storage of multiple potentiometer settings or data.

AC Timing Diagram



NOTE: MI REFERS TO THE MINIMUM INCREMENTAL CHANGE IN THE V_W OUTPUT DUE TO A CHANGE IN THE WIPER POSITION.

Pin Descriptions

R_H/V_H and R_L/V_L

The high (V_H/R_H) and low (V_L/R_L) terminals of the ISLX9C102, X9C103, X9C104, X9C503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. The terminology of V_H/R_H and V_L/R_L references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

R_W/V_W

V_W/R_W is the wiper terminal, and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in non-volatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the ISLX9C102, X9C103, X9C104, X9C503 device will be placed in the low power standby mode until the device is selected once again.

Principles of Operation

There are three sections of the X9C102, X9C103, ISL9C104 and ISL9C503: the input control, counter and decode section; the non-volatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions, the contents of the counter can be stored in non-volatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a "make-before-break" mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W/R_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the non-volatile memory. When power is restored, the contents of the memory are recalled and the wiper is reset to the value last stored.

The internal charge pump allows a wide range of voltages (from -5V to 5V) applied to XDCP terminals yet given a convenience of single power supply. The typical charge pump noise of 20mV at 850kHz should be taken in consideration when designing an application circuit.

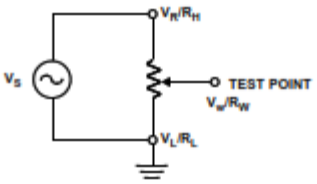
Electrical Specifications Over recommended operating conditions unless otherwise stated. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP (Note 6)	LIMITS MAX	UNIT
AC OPERATION CHARACTERISTICS						
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup		100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ Change		100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup		2.9			µs
t_{IL}	$\overline{INC}$ LOW Period		1			µs
t_{IH}	$\overline{INC}$ HIGH Period		1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive		1			µs
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)		20			ms
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)		100			ns
t_{IW} (5)	$\overline{INC}$ to $V_{W/RW}$ Change			100		µs
t_{CYC}	$\overline{INC}$ Cycle Time		2			µs
t_{CYC}	$\overline{INC}$ Input Rise and Fall Time				500	µs
t_R, t_F	Power-up to Wiper Stable (Note 7)			500		µs
t_{PU}	V_{CC} Power-up Rate (Note 7)		0.2		50	V/ms

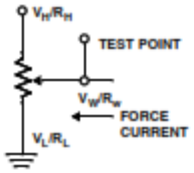
NOTES:

3. Absolute linearity is utilized to determine actual wiper voltage vs expected voltage = $[V_{W(n)(actual)} - V_{W(n)(expected)}] = \pm 1$ MI Maximum.
4. Relative linearity is a measure of the error in step size between taps = $V_{W(n+1)} - [V_{W(n)} + MI] = +0.2$ MI.
5. 1 MI = Minimum Increment = $R_{TOT}/99$.
6. Typical values are for $T_A = +25°C$ and nominal supply voltage.
7. This parameter is not 100% tested.

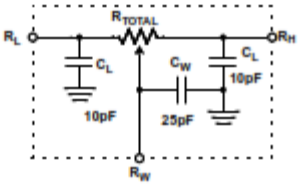
Test Circuit #1



Test Circuit #2



Circuit #3 SPICE Macro Model



Endurance and Data Retention

PARAMETER	MIN	UNIT
Medium Endurance	100,000	Data changes per bit per register
Data Retention	100	years

AC Conditions of Test

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input Reference Levels	1.5V

Power-up and Down Requirements

At all times, voltages on the potentiometer pins must be less than $\pm V_{CC}$. The recall of the wiper position from non-volatile memory is not in effect until the V_{CC} supply reaches its final value. The V_{CC} ramp rate specification is always in effect.

Absolute Maximum Ratings

Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC} with Respect to V_{SS} . . -1V to +7V
Voltage on V_H/R_H and V_L/R_L Referenced to V_{SS} . . . . . -5V to +5V
$\Delta V = |V_H/R_H - V_L/R_L|$
X9C102 . . . . . .4V
X9C103, X9C104, and X9C503 . . . . . .10V
I_W (10s) . . . . . .±6mA
Power Rating
X9C102 . . . . . .16mW
X9C103 X0C104, and X9C503 . . . . . .10mW

Thermal Information

Temperature Under Bias . . . . . .-65°C to +135°C
Storage Temperature . . . . . .-65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Recommended Operating Conditions

Commercial Temperature Range. . . . . 0°C to +70°C
Industrial Temperature Range . . . . . -40°C to +85°C
Supply Voltage Range (V_{CC}) . . . . . 5V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Electrical Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP (Note 6)	LIMITS MAX	UNIT
POTENTIOMETER CHARACTERISTICS						
R_{TOTAL}	End-to-End Resistance Variation		-20		+20	%
$V_{VH/RH}$	V_H Terminal Voltage		-5		+5	V
$V_{VL/RL}$	V_L Terminal Voltage		-5		+5	V
I_W	Wiper Current		-4.4		4.4	mA
R_W	Wiper Resistance	Wiper Current = ±1mA		40	100	Ω
	Resistor Noise (Note 7)	Ref 1kHz		-120		dBV
	Charge Pump Noise (Note 7)	@ 650kHz		20		mV_{RMS}
	Resolution			1		%
	Absolute Linearity (Note 3)	$V_{W(n)(actual)} - V_{W(n)(EXPECTED)}$	-1		+1	MI (Note 5)
	Relative Linearity (Note 4)	$V_{W(n+1)(ACTUAL)} - [V_{W(n)} + MI]$	-0.2		+0.2	MI (Note 5)
	R_{TOTAL} Temperature Coefficient	X9C103, X9C503, X9C104		±300 (Note 7)		ppm/°C
	R_{TOTAL} Temperature Coefficient	X9C102		±600 (Note 7)		ppm/°C
	Ratiometric Temperature Coefficient			±20		ppm/°C
$C_H/C_L/C_W$ (Note 7)	Potentiometer Capacitances	See "Circuit #3 SPICE Macro Model" on page 5.		10/10/25		pF
DC OPERATING CHARACTERISTICS						
I_{CC}	V_{CC} Active Current	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V to 2.4V at Max t_{CYC}		1	3	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ = V_{CC} - 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} - 0.3V		200	750	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current	V_{IN} = V_{SS} to V_{CC}			±10	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input HIGH Voltage		2			V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input LOW Voltage				0.8	V
C_{IN}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance (Note 7)	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = +25°C, f = 1MHz		10		pF

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	$\overline{INC}$	**INCREMENT** The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.
2	U/$\overline{D}$	**UP/DOWN** The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.
3	V_H/R_H	**V_H/R_H** The high (V_H/R_H) terminals of the X9C102, X9C103, X9C104, X9C503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. The terminology of V_H/R_H and V_L/R_L references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.
4	V_{SS}	**V_{SS}**
5	V_W/R_W	**V_W/R_W** V_W/R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.
6	R_L/V_L	**R_L/V_L** The low (V_L/R_L) terminals of the X9C102, X9C103, X9C104, X9C503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. The terminology of V_H/R_H and V_L/R_L references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.
7	$\overline{CS}$	**$\overline{CS}$** The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in non-volatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9C102, X9C103, X9C104, X9C503 device will be placed in the low power standby mode until the device is selected once again.
8	V_{CC}	**V_{CC}**

Ordering Information

PART NUMBER	PART MARKING	R_{TOTAL} (kΩ)	TEMP RANGE (°C)	PACKAGE	PACKAGE DWG. #
X9C102P	X9C102P	1	0 to +70	8 Ld PDIP	MDP0031
X9C102PZ (Notes 1, 2)	X9C102P Z		0 to +70	8 Ld PDIP (Pb-free)	MDP0031
X9C102PI	X9C102P I		-40 to +85	8 Ld PDIP	MDP0031
X9C102PIZ (Notes 1, 2)	X9C102P ZI		-40 to +85	8 Ld PDIP (Pb-free)	MDP0031
X9C102S*, **	X9C102S		0 to +70	8 Ld SOIC	MDP0027
X9C102SZ* (Note 1)	X9C102S Z		0 to +70	8 Ld SOIC (Pb-free)	MDP0027
X9C102SI*, **	X9C102S I		-40 to +85	8 Ld SOIC	MDP0027
X9C102SIZ*, ** (Note 1)	X9C102S ZI		-40 to +85	8 Ld SOIC (Pb-free)	MDP0027
X9C103P	X9C103P	10	0 to +70	8 Ld PDIP	MDP0031
X9C103PZ (Notes 1, 2)	X9C103P Z		0 to +70	8 Ld PDIP (Pb-free)	MDP0031
X9C103PI	X9C103P I		-40 to +85	8 Ld PDIP	MDP0031
X9C103PIZ (Note 1)	X9C103P ZI		-40 to +85	8 Ld PDIP (Pb-free)	MDP0031
X9C103S*, **	X9C103S		0 to +70	8 Ld SOIC	MDP0027
X9C103SZ*, ** (Note 1)	X9C103S Z		0 to +70	8 Ld SOIC (Pb-free)	MDP0027
X9C103SI*, **	X9C103S I		-40 to +85	8 Ld SOIC	MDP0027
X9C103SIZ*, ** (Note 1)	X9C103S ZI		-40 to +85	8 Ld SOIC (Pb-free)	MDP0027
X9C503P	X9C503P	50	0 to +70	8 Ld PDIP	MDP0031
X9C503PZ (Notes 1, 2)	X9C503P Z		0 to +70	8 Ld PDIP (Pb-free)	MDP0031
X9C503PI	X9C503P I		-40 to +85	8 Ld PDIP	MDP0031
X9C503PIZ (Notes 1, 2)	X9C503P ZI		-40 to +85	8 Ld PDIP (Pb-free)	MDP0031
X9C503S*	X9C503S		0 to +70	8 Ld SOIC	MDP0027
X9C503SZ* (Note 1)	X9C503S Z		0 to +70	8 Ld SOIC (Pb-free)	MDP0027
X9C503SI*, **	X9C503S I		-40 to +85	8 Ld SOIC	MDP0027
X9C503SIZ*, ** (Note 1)	X9C503S ZI		-40 to +85	8 Ld SOIC (Pb-free)	MDP0027
X9C104P	X9C104P	100	0 to +70	8 Ld PDIP	MDP0031
X9C104PI	X9C104P I		-40 to +85	8 Ld PDIP	MDP0031
X9C104PIZ (Notes 1, 2)	X9C104P ZI		-40 to +85	8 Ld PDIP (Pb-free)	MDP0031
X9C104S*, **	X9C104S		0 to +70	8 Ld SOIC	MDP0027
X9C104SZ*, ** (Note 1)	X9C104S Z		0 to +70	8 Ld SOIC (Pb-free)	MDP0027
X9C104SI*, **	X9C104S I		-40 to +85	8 Ld SOIC	MDP0027
X9C104SIZ*, ** (Note 1)	X9C104S ZI		-40 to +85	8 Ld SOIC (Pb-free)	MDP0027

*Add "T1" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

**Add "T2" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Data Sheet | July 20, 2009 | FN8222.3

Digitally Controlled Potentiometer (XDCP™)

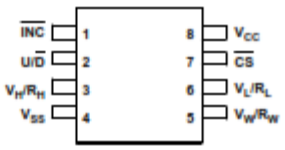
The X9C102, X9C103, X9C104, X9C503 are Intersils' digitally controlled (XDCP) potentiometers. The device consists of a resistor array, wiper switches, a control section, and non-volatile memory. The wiper position is controlled by a three-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in non-volatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications ranging from control to signal processing to parameter adjustment.

Pinout

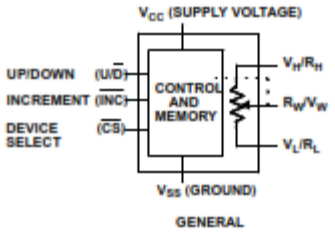
X9C102, X9C103, X9C104, X9C503
(8 LD SOIC, 8 LD PDIP)
TOP VIEW

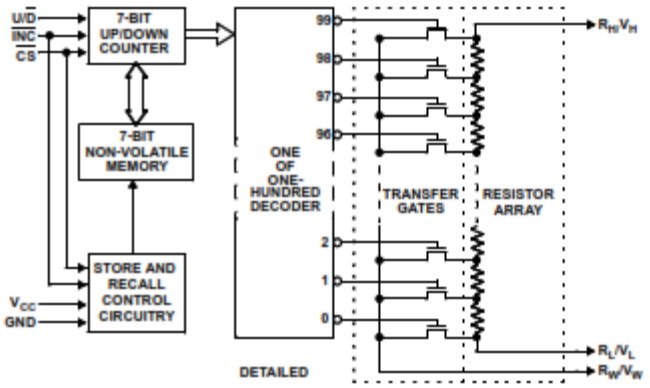


Features

- Solid-State Potentiometer
- Three-Wire Serial Interface
- 100 Wiper Tap Points
  - Wiper Position Stored in Non-volatile Memory and Recalled on Power-up
- 99 Resistive Elements
  - Temperature Compensated
  - End-to-End Resistance, ±20%
  - Terminal Voltages, ±5V
- Low Power CMOS
  - V_{CC} = 5V
  - Active Current, 3mA max.
  - Standby Current, 750µA max.
- High Reliability
  - Endurance, 100,000 Data Changes per Bit
  - Register Data Retention, 100 years
- X9C102 = 1kΩ
- X9C103 = 10kΩ
- X9C503 = 50kΩ
- X9C104 = 100kΩ
- Packages
  - 8 Ld SOIC
  - 8 Ld PDIP
- Pb-Free Available (RoHS Compliant)

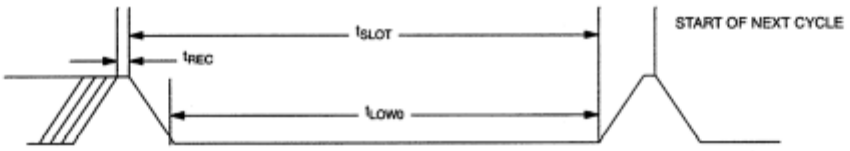
Block Diagram



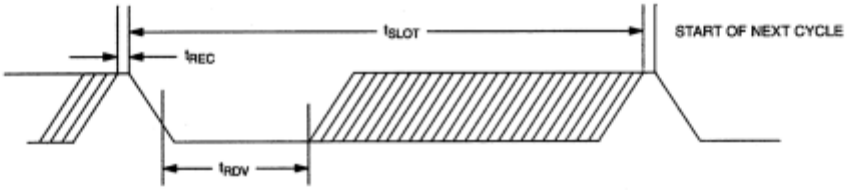


TIMING DIAGRAMS Figure 18

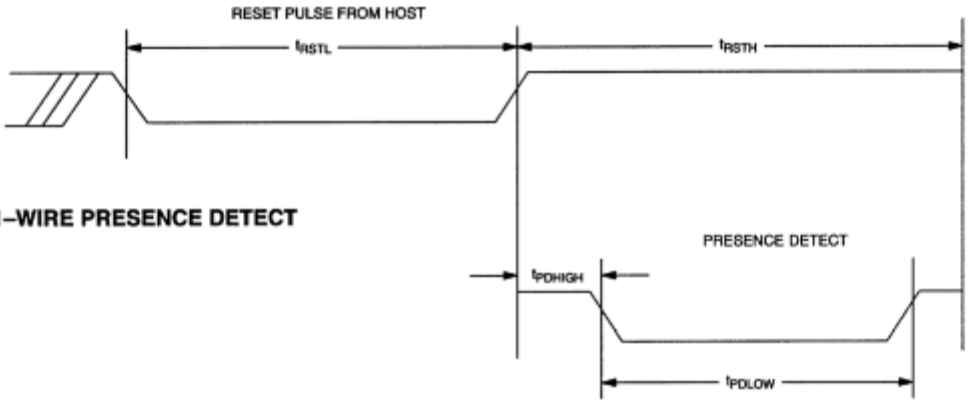
1–WIRE WRITE ZERO TIME SLOT



1–WIRE READ ZERO TIME SLOT



1–WIRE RESET PULSE



1–WIRE PRESENCE DETECT

AC ELECTRICAL CHARACTERISTICS: NV MEMORY

(-55°C to +100°C; V_{DD} = 3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
NV Write Cycle Time	t_{WR}			2	10	ms
EEPROM Writes	N_{EEWR}	-55°C to +55°C	50k			writes
EEPROM Data Retention	t_{EEDR}	-55°C to +55°C	10			years

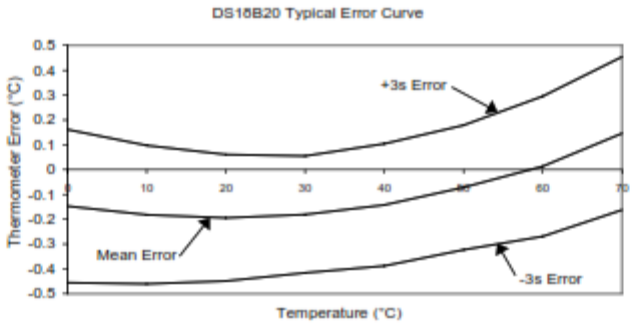
AC ELECTRICAL CHARACTERISTICS (-55°C to +125°C; V_{DD} = 3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}	9-bit resolution			93.75	ms	1
		10-bit resolution			187.5	ms	1
		11-bit resolution			375	ms	1
		12-bit resolution			750	ms	1
Time to Strong Pullup On	t_{SPON}	Start Convert T Command Issued			10	µs	
Time Slot	t_{SLOT}		60		120	µs	1
Recovery Time	t_{REC}		1			µs	1
Write 0 Low Time	t_{LOW0}		60		120	µs	1
Write 1 Low Time	t_{LOW1}		1		15	µs	1
Read Data Valid	t_{RDV}				15	µs	1
Reset Time High	t_{RSTH}		480			µs	1
Reset Time Low	t_{RSTL}		480			µs	1,2
Presence Detect High	t_{PDHIGH}		15		60	µs	1
Presence Detect Low	t_{PDLOW}		60		240	µs	1
Capacitance	$C_{IN/OUT}$				25	pF	

NOTES:

1) Refer to timing diagrams in Figure 18.
2) Under parasite power, if t_{RSTL} > 960µs, a power on reset may occur.

TYPICAL PERFORMANCE CURVE Figure 17



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +6.0V
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-55°C to +125°C
Solder Temperature	See IPC/JEDEC J-STD-020A

**These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

DC ELECTRICAL CHARACTERISTICS (-55°C to +125°C; V_{DD}=3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	Local Power	+3.0		+5.5	V	1
Pullup Supply Voltage	V_{PU}	Parasite Power	+3.0		+5.5	V	1,2
		Local Power	+3.0		V_{DD}		
Thermometer Error	t_{ERR}	-10°C to +85°C			±0.5	°C	3
		-55°C to +125°C			±2		
Input Logic Low	V_{IL}		-0.3		+0.8	V	1,4,5
Input Logic High	V_{IH}	Local Power	+2.2		The lower of 5.5 or V_{DD} + 0.3	V	1, 6
		Parasite Power	+3.0				
Sink Current	I_L	$V_{I/O}$=0.4V	4.0			mA	1
Standby Current	I_{DDS}			750	1000	nA	7,8
Active Current	I_{DD}	V_{DD}=5V		1	1.5	mA	9
DQ Input Current	I_{DQ}			5		µA	10
Drift				±0.2		°C	11

NOTES:

1) All voltages are referenced to ground.
2) The Pullup Supply Voltage specification assumes that the pullup device is ideal, and therefore the high level of the pullup is equal to V_{PU}. In order to meet the V_{IH} spec of the DS18B20, the actual supply rail for the strong pullup transistor must include margin for the voltage drop across the transistor when it is turned on; thus: $V_{PU\_ACTUAL} = V_{PU\_IDEAL} + V_{TRANSISTOR}$.
3) See typical performance curve in Figure 17
4) Logic low voltages are specified at a sink current of 4mA.
5) To guarantee a presence pulse under low voltage parasite power conditions, V_{ILMAX} may have to be reduced to as low as 0.5V.
6) Logic high voltages are specified at a source current of 1mA.
7) Standby current specified up to 70°C. Standby current typically is 3µA at 125°C.
8) To minimize I_{DDS}, DQ should be within the following ranges: GND ≤ DQ ≤ GND + 0.3V or V_{DD} − 0.3V ≤ DQ ≤ V_{DD}.
9) Active current refers to supply current during active temperature conversions or EEPROM writes.
10) DQ line is high ("hi-Z" state).
11) Drift data is based on a 1000 hour stress test at 125°C with V_{DD} = 5.5V.

DS18B20 OPERATION EXAMPLE 1

In this example there are multiple DS18B20s on the bus and they are using parasite power. The bus master initiates a temperature conversion in a specific DS18B20 and then reads its scratchpad and recalculates the CRC to verify the data.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Master issues reset pulse.
RX	Presence	DS18B20s respond with presence pulse.
TX	55h	Master issues Match ROM command.
TX	64-bit ROM code	Master sends DS18B20 ROM code.
TX	44h	Master issues Convert T command.
TX	DQ line held high by strong pullup	Master applies strong pullup to DQ for the duration of the conversion (t_{conv}).
TX	Reset	Master issues reset pulse.
RX	Presence	DS18B20s respond with presence pulse.
TX	55h	Master issues Match ROM command.
TX	64-bit ROM code	Master sends DS18B20 ROM code.
TX	BEh	Master issues Read Scratchpad command.
RX	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.

DS18B20 OPERATION EXAMPLE 2

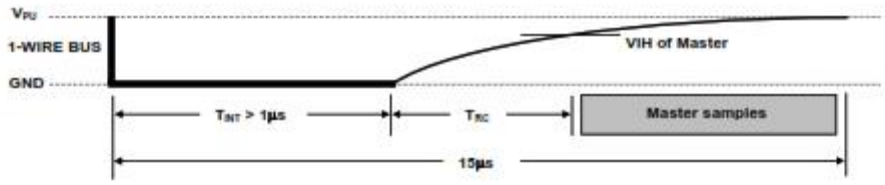
In this example there is only one DS18B20 on the bus and it is using parasite power. The master writes to the T_H, T_L, and configuration registers in the DS18B20 scratchpad and then reads the scratchpad and recalculates the CRC to verify the data. The master then copies the scratchpad contents to EEPROM.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Master issues reset pulse.
RX	Presence	DS18B20 responds with presence pulse.
TX	CCh	Master issues Skip ROM command.
TX	4Eh	Master issues Write Scratchpad command.
TX	3 data bytes	Master sends three data bytes to scratchpad (T_H, T_L, and config).
TX	Reset	Master issues reset pulse.
RX	Presence	DS18B20 responds with presence pulse.
TX	CCh	Master issues Skip ROM command.
TX	BEh	Master issues Read Scratchpad command.
RX	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.
TX	Reset	Master issues reset pulse.
RX	Presence	DS18B20 responds with presence pulse.
TX	CCh	Master issues Skip ROM command.
TX	48h	Master issues Copy Scratchpad command.
TX	DQ line held high by strong pullup	Master applies strong pullup to DQ for at least 10ms while copy operation is in progress.

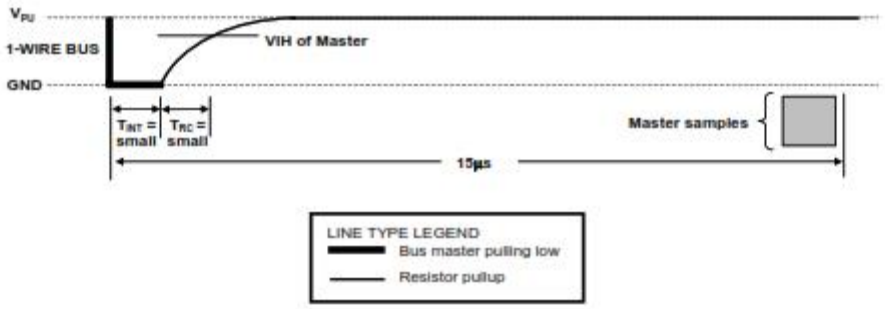
data from the DS18B20 is valid for 15µs after the falling edge that initiated the read time slot. Therefore, the master must release the bus and then sample the bus state within 15µs from the start of the slot.

Figure 15 illustrates that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs for a read time slot. Figure 16 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as short as possible and by locating the master sample time during read time slots towards the end of the 15µs period.

DETAILED MASTER READ 1 TIMING Figure 15



RECOMMENDED MASTER READ 1 TIMING Figure 16



RELATED APPLICATION NOTES

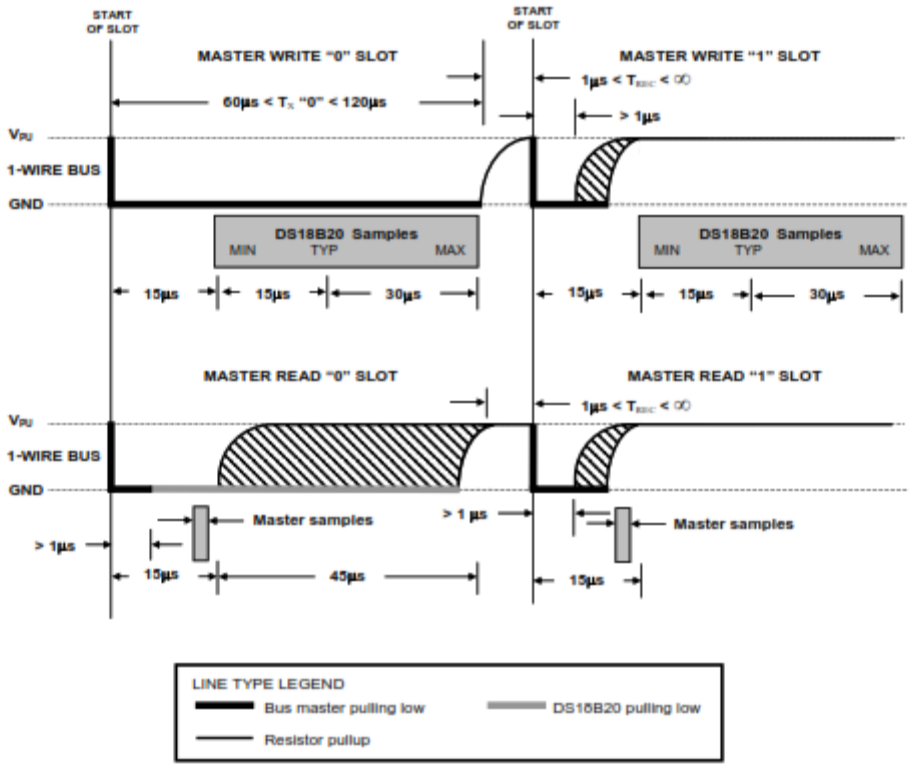
The following Application Notes can be applied to the DS18B20. These notes can be obtained from the Maxim website at http://www.maxim-ic.com, or through our faxback service at (214) 450–0441.

Application Note 27: Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Product
Application Note 122: Using Dallas' 1-Wire ICs in 1-Cell Li-Ion Battery Packs with Low-Side N-Channel Safety FETs Master
Application Note 126: 1-Wire Communication Through Software
Application Note 162: Interfacing the DS18X20/DS1822 1-Wire Temperature Sensor in a Microcontroller Environment
App Note 208: Curve Fitting the Error of a Bandgap-Based Digital Temperature Sensor
App Note 2420: 1-Wire Communication with a Microchip PICmicro Microcontroller
App Note 3754: Single-Wire Serial Bus Carries Isolated Power and Data

Sample 1-Wire subroutines that can be used in conjunction with AN74 can be downloaded from the Maxim website.

The DS18B20 samples the 1-Wire bus during a window that lasts from 15µs to 60µs after the master initiates the write time slot. If the bus is high during the sampling window, a 1 is written to the DS18B20. If the line is low, a 0 is written to the DS18B20.

READ/WRITE TIME SLOT TIMING DIAGRAM Figure 14



READ TIME SLOTS

The DS18B20 can only transmit data to the master when the master issues read time slots. Therefore, the master must generate read time slots immediately after issuing a Read Scratchpad [BEh] or Read Power Supply [B4h] command, so that the DS18B20 can provide the requested data. In addition, the master can generate read time slots after issuing Convert T [44h] or Recall E^2 [B8h] commands to find out the status of the operation as explained in the *DS18B20 FUNCTION COMMAND* section.

All read time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between slots. A read time slot is initiated by the master device pulling the 1-Wire bus low for a minimum of 1µs and then releasing the bus (see Figure 14). After the master initiates the read time slot, the DS18B20 will begin transmitting a 1 or 0 on bus. The DS18B20 transmits a 1 by leaving the bus high and transmits a 0 by pulling the bus low. When transmitting a 0, the DS18B20 will release the bus by the end of the time slot, and the bus will be pulled back to its high idle state by the pullup resister. Output

1-WIRE SIGNALING

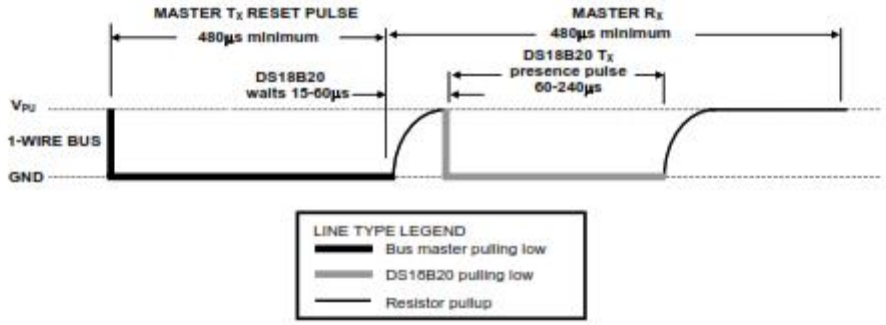
The DS18B20 uses a strict 1-Wire communication protocol to insure data integrity. Several signal types are defined by this protocol: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. The bus master initiates all of these signals, with the exception of the presence pulse.

INITIALIZATION PROCEDURE: RESET AND PRESENCE PULSES

All communication with the DS18B20 begins with an initialization sequence that consists of a reset pulse from the master followed by a presence pulse from the DS18B20. This is illustrated in Figure 13. When the DS18B20 sends the presence pulse in response to the reset, it is indicating to the master that it is on the bus and ready to operate.

During the initialization sequence the bus master transmits (T_X) the reset pulse by pulling the 1-Wire bus low for a minimum of 480µs. The bus master then releases the bus and goes into receive mode (R_X). When the bus is released, the 5k pullup resistor pulls the 1-Wire bus high. When the DS18B20 detects this rising edge, it waits 15µs to 60µs and then transmits a presence pulse by pulling the 1-Wire bus low for 60µs to 240µs.

INITIALIZATION TIMING Figure 13



READ/WRITE TIME SLOTS

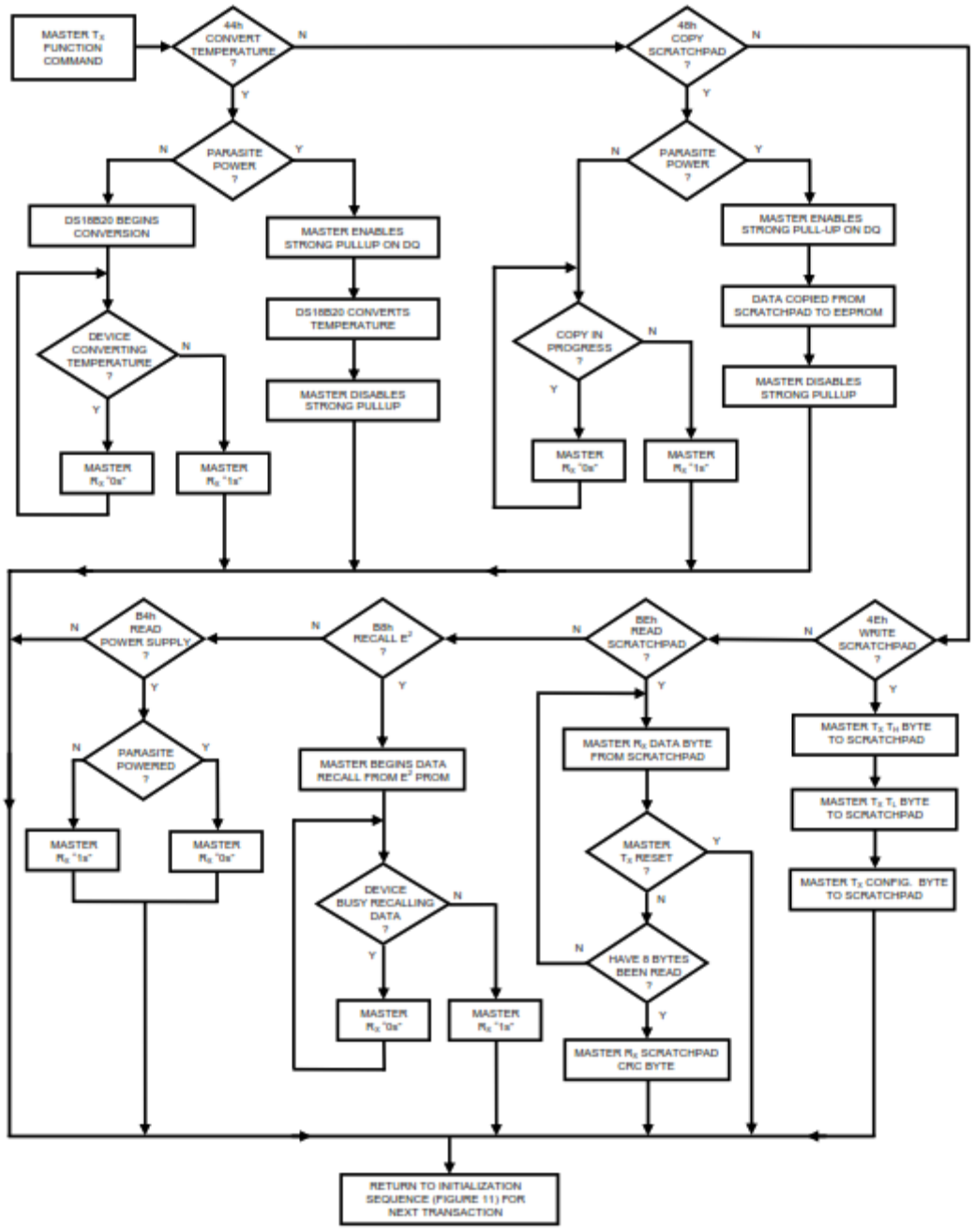
The bus master writes data to the DS18B20 during write time slots and reads data from the DS18B20 during read time slots. One bit of data is transmitted over the 1-Wire bus per time slot.

WRITE TIME SLOTS

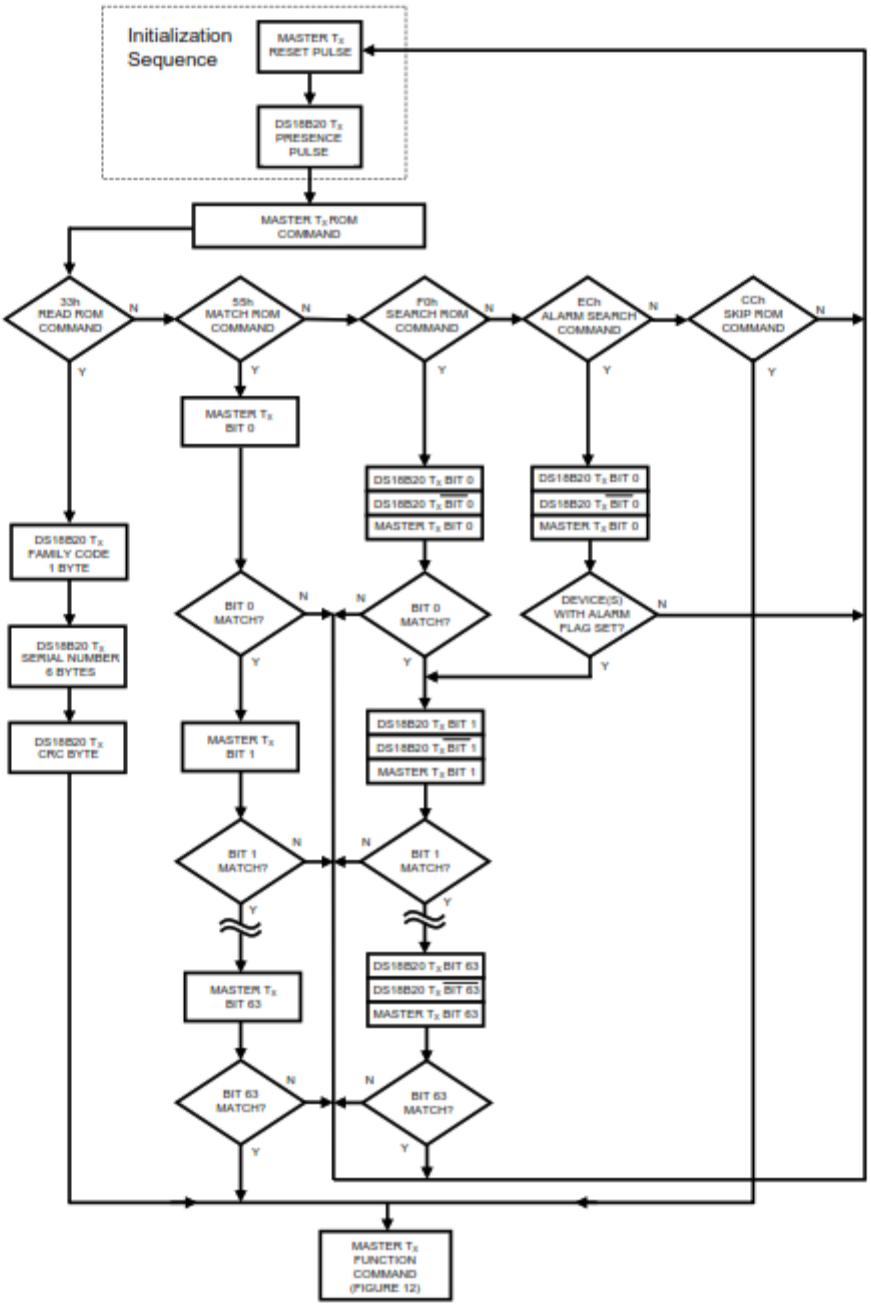
There are two types of write time slots: "Write 1" time slots and "Write 0" time slots. The bus master uses a Write 1 time slot to write a logic 1 to the DS18B20 and a Write 0 time slot to write a logic 0 to the DS18B20. All write time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between individual write slots. Both types of write time slots are initiated by the master pulling the 1-Wire bus low (see Figure 14).

To generate a Write 1 time slot, after pulling the 1-Wire bus low, the bus master must release the 1-Wire bus within 15µs. When the bus is released, the 5k pullup resistor will pull the bus high. To generate a Write 0 time slot, after pulling the 1-Wire bus low, the bus master must continue to hold the bus low for the duration of the time slot (at least 60µs).

DS18B20 FUNCTION COMMANDS FLOW CHART Figure 12



ROM COMMANDS FLOW CHART Figure 11



COPY SCRATCHPAD [48h]

This command copies the contents of the scratchpad T_H, T_L and configuration registers (bytes 2, 3 and 4) to EEPROM. If the device is being used in parasite power mode, within 10µs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for at least 10ms as described in the *POWERING THE DS18B20* section.

RECALL E^2 [B8h]

This command recalls the alarm trigger values (T_H and T_L) and configuration data from EEPROM and places the data in bytes 2, 3, and 4, respectively, in the scratchpad memory. The master device can issue read time slots following the Recall E^2 command and the DS18B20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done. The recall operation happens automatically at power-up, so valid data is available in the scratchpad as soon as power is applied to the device.

READ POWER SUPPLY [B4h]

The master device issues this command followed by a read time slot to determine if any DS18B20s on the bus are using parasite power. During the read time slot, parasite powered DS18B20s will pull the bus low, and externally powered DS18B20s will let the bus remain high. Refer to the *POWERING THE DS18B20* section for usage information for this command.

DS18B20 FUNCTION COMMAND SET Table 4

Command	Description	Protocol	1-Wire Bus Activity After Command is Issued	Notes
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	DS18B20 transmits conversion status to master (not applicable for parasite-powered DS18B20s).	1
MEMORY COMMANDS				
Read Scratchpad	Reads the entire scratchpad including the CRC byte.	BEh	DS18B20 transmits up to 9 data bytes to master.	2
Write Scratchpad	Writes data into scratchpad bytes 2, 3, and 4 (T_H, T_L, and configuration registers).	4Eh	Master transmits 3 data bytes to DS18B20.	3
Copy Scratchpad	Copies T_H, T_L, and configuration register data from the scratchpad to EEPROM.	48h	None	1
Recall E^2	Recalls T_H, T_L, and configuration register data from EEPROM to the scratchpad.	B8h	DS18B20 transmits recall status to master.	
Read Power Supply	Signals DS18B20 power supply mode to the master.	B4h	DS18B20 transmits supply status to master.	

NOTES:

1) For parasite-powered DS18B20s, the master must enable a strong pullup on the 1-Wire bus during temperature conversions and copies from the scratchpad to EEPROM. No other bus activity may take place during this time.
2) The master can interrupt the transmission of data at any time by issuing a reset.
3) All three bytes must be written before a reset is issued.

SKIP ROM [CCh]

The master can use this command to address all devices on the bus simultaneously without sending out any ROM code information. For example, the master can make all DS18B20s on the bus perform simultaneous temperature conversions by issuing a Skip ROM command followed by a Convert T [44h] command.

Note that the Read Scratchpad [BEh] command can follow the Skip ROM command only if there is a single slave device on the bus. In this case time is saved by allowing the master to read from the slave without sending the device's 64-bit ROM code. A Skip ROM command followed by a Read Scratchpad command will cause a data collision on the bus if there is more than one slave since multiple devices will attempt to transmit data simultaneously.

ALARM SEARCH [ECh]

The operation of this command is identical to the operation of the Search ROM command except that only slaves with a set alarm flag will respond. This command allows the master device to determine if any DS18B20s experienced an alarm condition during the most recent temperature conversion. After every Alarm Search cycle (i.e., Alarm Search command followed by data exchange), the bus master must return to Step 1 (Initialization) in the transaction sequence. Refer to the *OPERATION — ALARM SIGNALING* section for an explanation of alarm flag operation.

DS18B20 FUNCTION COMMANDS

After the bus master has used a ROM command to address the DS18B20 with which it wishes to communicate, the master can issue one of the DS18B20 function commands. These commands allow the master to write to and read from the DS18B20's scratchpad memory, initiate temperature conversions and determine the power supply mode. The DS18B20 function commands, which are described below, are summarized in Table 4 and illustrated by the flowchart in Figure 12.

CONVERT T [44h]

This command initiates a single temperature conversion. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the DS18B20 returns to its low-power idle state. If the device is being used in parasite power mode, within 10µs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for the duration of the conversion (t_{conv}) as described in the *POWERING THE DS18B20* section. If the DS18B20 is powered by an external supply, the master can issue read time slots after the Convert T command and the DS18B20 will respond by transmitting a 0 while the temperature conversion is in progress and a 1 when the conversion is done. In parasite power mode this notification technique cannot be used since the bus is pulled high by the strong pullup during the conversion.

WRITE SCRATCHPAD [4Eh]

This command allows the master to write 3 bytes of data to the DS18B20's scratchpad. The first data byte is written into the T_H register (byte 2 of the scratchpad), the second byte is written into the T_L register (byte 3), and the third byte is written into the configuration register (byte 4). Data must be transmitted least significant bit first. All three bytes MUST be written before the master issues a reset, or the data may be corrupted.

READ SCRATCHPAD [BEh]

This command allows the master to read the contents of the scratchpad. The data transfer starts with the least significant bit of byte 0 and continues through the scratchpad until the 9th byte (byte 8 – CRC) is read. The master may issue a reset to terminate reading at any time if only part of the scratchpad data is needed.

TRANSACTION SEQUENCE

The transaction sequence for accessing the DS18B20 is as follows:

Step 1. Initialization

Step 2. ROM Command (followed by any required data exchange)

Step 3. DS18B20 Function Command (followed by any required data exchange)

It is very important to follow this sequence every time the DS18B20 is accessed, as the DS18B20 will not respond if any steps in the sequence are missing or out of order. Exceptions to this rule are the Search ROM [F0h] and Alarm Search [ECh] commands. After issuing either of these ROM commands, the master must return to Step 1 in the sequence.

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that slave devices (such as the DS18B20) are on the bus and are ready to operate. Timing for the reset and presence pulses is detailed in the *1-WIRE SIGNALING* section.

ROM COMMANDS

After the bus master has detected a presence pulse, it can issue a ROM command. These commands operate on the unique 64-bit ROM codes of each slave device and allow the master to single out a specific device if many are present on the 1-Wire bus. These commands also allow the master to determine how many and what types of devices are present on the bus or if any device has experienced an alarm condition. There are five ROM commands, and each command is 8 bits long. The master device must issue an appropriate ROM command before issuing a DS18B20 function command. A flowchart for operation of the ROM commands is shown in Figure 11.

SEARCH ROM [F0h]

When a system is initially powered up, the master must identify the ROM codes of all slave devices on the bus, which allows the master to determine the number of slaves and their device types. The master learns the ROM codes through a process of elimination that requires the master to perform a Search ROM cycle (i.e., Search ROM command followed by data exchange) as many times as necessary to identify all of the slave devices. If there is only one slave on the bus, the simpler Read ROM command (see below) can be used in place of the Search ROM process. For a detailed explanation of the Search ROM procedure, refer to the *iButton® Book of Standards* at www.ibutton.com/ibuttons/standard.pdf. After every Search ROM cycle, the bus master must return to Step 1 (Initialization) in the transaction sequence.

READ ROM [33h]

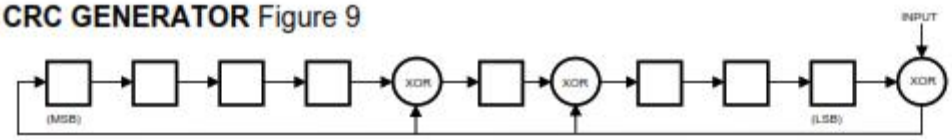
This command can only be used when there is one slave on the bus. It allows the bus master to read the slave's 64-bit ROM code without using the Search ROM procedure. If this command is used when there is more than one slave present on the bus, a data collision will occur when all the slaves attempt to respond at the same time.

MATCH ROM [55h]

The match ROM command followed by a 64-bit ROM code sequence allows the bus master to address a specific slave device on a multidrop or single-drop bus. Only the slave that exactly matches the 64-bit ROM code sequence will respond to the function command issued by the master; all other slaves on the bus will wait for a reset pulse.

is available in *Application Note 27: Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products*.

CRC GENERATOR Figure 9



1-WIRE BUS SYSTEM

The 1-Wire bus system uses a single bus master to control one or more slave devices. The DS18B20 is always a slave. When there is only one slave on the bus, the system is referred to as a "single-drop" system; the system is "multidrop" if there are multiple slaves on the bus.

All data and commands are transmitted least significant bit first over the 1-Wire bus.

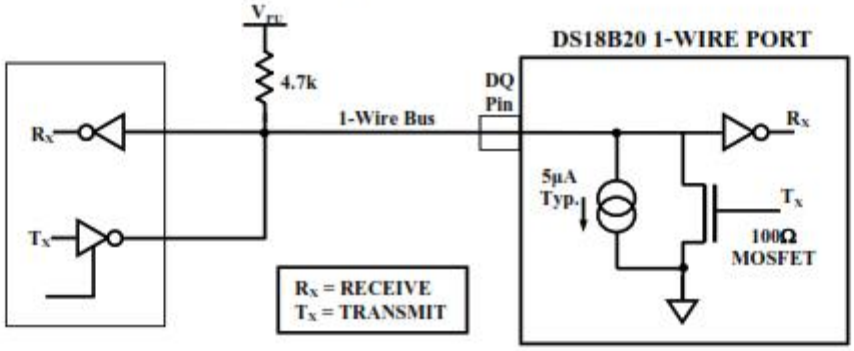
The following discussion of the 1-Wire bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1-Wire bus has by definition only a single data line. Each device (master or slave) interfaces to the data line via an open-drain or 3-state port. This allows each device to "release" the data line when the device is not transmitting data so the bus is available for use by another device. The 1-Wire port of the DS18B20 (the DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 10.

The 1-Wire bus requires an external pullup resistor of approximately 5kΩ; thus, the idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If the bus is held low for more than 480μs, all components on the bus will be reset.

HARDWARE CONFIGURATION Figure 10



CONFIGURATION REGISTER

Byte 4 of the scratchpad memory contains the configuration register, which is organized as illustrated in Figure 8. The user can set the conversion resolution of the DS18B20 using the R0 and R1 bits in this register as shown in Table 3. The power-up default of these bits is R0 = 1 and R1 = 1 (12-bit resolution). Note that there is a direct tradeoff between resolution and conversion time. Bit 7 and bits 0 to 4 in the configuration register are reserved for internal use by the device and cannot be overwritten.

CONFIGURATION REGISTER Figure 8

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	R1	R0	1	1	1	1	1

THERMOMETER RESOLUTION CONFIGURATION Table 3

R1	R0	Resolution	Max Conversion Time	
0	0	9-bit	93.75 ms	(t_{CONV}/8)
0	1	10-bit	187.5 ms	(t_{CONV}/4)
1	0	11-bit	375 ms	(t_{CONV}/2)
1	1	12-bit	750 ms	(t_{CONV})

CRC GENERATION

CRC bytes are provided as part of the DS18B20's 64-bit ROM code and in the 9th byte of the scratchpad memory. The ROM code CRC is calculated from the first 56 bits of the ROM code and is contained in the most significant byte of the ROM. The scratchpad CRC is calculated from the data stored in the scratchpad, and therefore it changes when the data in the scratchpad changes. The CRCs provide the bus master with a method of data validation when data is read from the DS18B20. To verify that data has been read correctly, the bus master must re-calculate the CRC from the received data and then compare this value to either the ROM code CRC (for ROM reads) or to the scratchpad CRC (for scratchpad reads). If the calculated CRC matches the read CRC, the data has been received error free. The comparison of CRC values and the decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS18B20 that prevents a command sequence from proceeding if the DS18B20 CRC (ROM or scratchpad) does not match the value generated by the bus master.

The equivalent polynomial function of the CRC (ROM or scratchpad) is:

$$CRC = X^8 + X^5 + X^4 + 1$$

The bus master can re-calculate the CRC and compare it to the CRC values from the DS18B20 using the polynomial generator shown in Figure 9. This circuit consists of a shift register and XOR gates, and the shift register bits are initialized to 0. Starting with the least significant bit of the ROM code or the least significant bit of byte 0 in the scratchpad, one bit at a time should shifted into the shift register. After shifting in the 56th bit from the ROM or the most significant bit of byte 7 from the scratchpad, the polynomial generator will contain the re-calculated CRC. Next, the 8-bit ROM code or scratchpad CRC from the DS18B20 must be shifted into the circuit. At this point, if the re-calculated CRC was correct, the shift register will contain all 0s. Additional information about the Dallas 1-Wire cyclic redundancy check

MEMORY

The DS18B20's memory is organized as shown in Figure 7. The memory consists of an SRAM scratchpad with nonvolatile EEPROM storage for the high and low alarm trigger registers (T_H and T_L) and configuration register. Note that if the DS18B20 alarm function is not used, the T_H and T_L registers can serve as general-purpose memory. All memory commands are described in detail in the *DS18B20 FUNCTION COMMANDS* section.

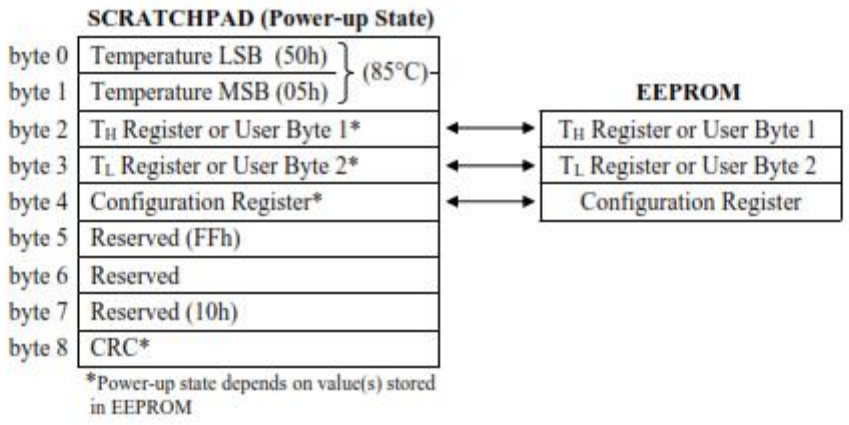
Byte 0 and byte 1 of the scratchpad contain the LSB and the MSB of the temperature register, respectively. These bytes are read-only. Bytes 2 and 3 provide access to T_H and T_L registers. Byte 4 contains the configuration register data, which is explained in detail in the CONFIGURATION REGISTER section of this datasheet. Bytes 5, 6, and 7 are reserved for internal use by the device and cannot be overwritten.

Byte 8 of the scratchpad is read-only and contains the cyclic redundancy check (CRC) code for bytes 0 through 7 of the scratchpad. The DS18B20 generates this CRC using the method described in *the CRC GENERATION* section.

Data is written to bytes 2, 3, and 4 of the scratchpad using the Write Scratchpad [4Eh] command; the data must be transmitted to the DS18B20 starting with the least significant bit of byte 2. To verify data integrity, the scratchpad can be read (using the Read Scratchpad [BEh] command) after the data is written. When reading the scratchpad, data is transferred over the 1-Wire bus starting with the least significant bit of byte 0. To transfer the T_H, T_L and configuration data from the scratchpad to EEPROM, the master must issue the Copy Scratchpad [48h] command.

Data in the EEPROM registers is retained when the device is powered down; at power-up the EEPROM data is reloaded into the corresponding scratchpad locations. Data can also be reloaded from EEPROM to the scratchpad at any time using the Recall E^2 [B8h] command. The master can issue read time slots following the Recall E^2 command and the DS18B20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done.

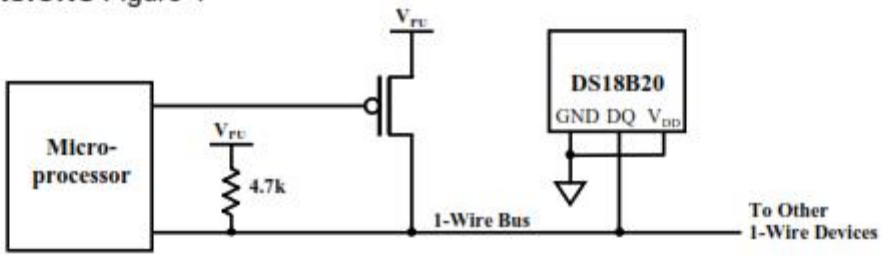
DS18B20 MEMORY MAP Figure 7



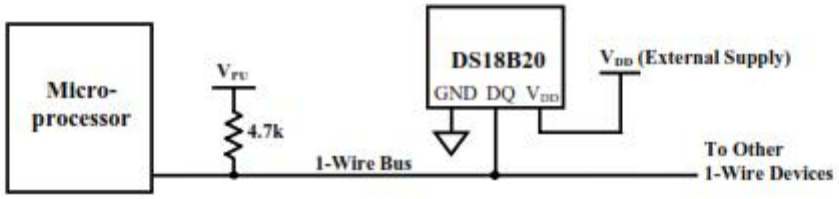
The use of parasite power is not recommended for temperatures above +100°C since the DS18B20 may not be able to sustain communications due to the higher leakage currents that can exist at these temperatures. For applications in which such temperatures are likely, it is strongly recommended that the DS18B20 be powered by an external power supply.

In some situations the bus master may not know whether the DS18B20s on the bus are parasite powered or powered by external supplies. The master needs this information to determine if the strong bus pullup should be used during temperature conversions. To get this information, the master can issue a Skip ROM [CCh] command followed by a Read Power Supply [B4h] command followed by a "read time slot". During the read time slot, parasite powered DS18B20s will pull the bus low, and externally powered DS18B20s will let the bus remain high. If the bus is pulled low, the master knows that it must supply the strong pullup on the 1-Wire bus during temperature conversions.

SUPPLYING THE PARASITE-POWERED DS18B20 DURING TEMPERATURE CONVERSIONS Figure 4



POWERING THE DS18B20 WITH AN EXTERNAL SUPPLY Figure 5



64-BIT LASERED ROM CODE

Each DS18B20 contains a unique 64–bit code (see Figure 6) stored in ROM. The least significant 8 bits of the ROM code contain the DS18B20's 1-Wire family code: 28h. The next 48 bits contain a unique serial number. The most significant 8 bits contain a cyclic redundancy check (CRC) byte that is calculated from the first 56 bits of the ROM code. A detailed explanation of the CRC bits is provided in the *CRC GENERATION* section. The 64-bit ROM code and associated ROM function control logic allow the DS18B20 to operate as a 1-Wire device using the protocol detailed in the *1-WIRE BUS SYSTEM* section of this datasheet.

64-BIT LASERED ROM CODE Figure 6

8-BIT CRC		48-BIT SERIAL NUMBER		8-BIT FAMILY CODE (28h)	
MSB	LSB	MSB	LSB	MSB	LSB

OPERATION — ALARM SIGNALING

After the DS18B20 performs a temperature conversion, the temperature value is compared to the user-defined two's complement alarm trigger values stored in the 1-byte T_H and T_L registers (see Figure 3). The sign bit (S) indicates if the value is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. The T_H and T_L registers are nonvolatile (EEPROM) so they will retain data when the device is powered down. T_H and T_L can be accessed through bytes 2 and 3 of the scratchpad as explained in the *MEMORY* section of this datasheet.

T_H AND T_L REGISTER FORMAT Figure 3

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
S	2^6	2^5	2^5	2^5	2^2	2^1	2^0

Only bits 11 through 4 of the temperature register are used in the T_H and T_L comparison since T_H and T_L are 8-bit registers. If the measured temperature is lower than or equal to T_L or higher than or equal to T_H, an alarm condition exists and an alarm flag is set inside the DS18B20. This flag is updated after every temperature measurement; therefore, if the alarm condition goes away, the flag will be turned off after the next temperature conversion.

The master device can check the alarm flag status of all DS18B20s on the bus by issuing an Alarm Search [ECh] command. Any DS18B20s with a set alarm flag will respond to the command, so the master can determine exactly which DS18B20s have experienced an alarm condition. If an alarm condition exists and the T_H or T_L settings have changed, another temperature conversion should be done to validate the alarm condition.

POWERING THE DS18B20

The DS18B20 can be powered by an external supply on the V_{DD} pin, or it can operate in "parasite power" mode, which allows the DS18B20 to function without a local external supply. Parasite power is very useful for applications that require remote temperature sensing or that are very space constrained. Figure 1 shows the DS18B20's parasite-power control circuitry, which "steals" power from the 1-Wire bus via the DQ pin when the bus is high. The stolen charge powers the DS18B20 while the bus is high, and some of the charge is stored on the parasite power capacitor (C_{PP}) to provide power when the bus is low. When the DS18B20 is used in parasite power mode, the V_{DD} pin must be connected to ground.
In parasite power mode, the 1-Wire bus and C_{PP} can provide sufficient current to the DS18B20 for most operations as long as the specified timing and voltage requirements are met (refer to *the DC ELECTRICAL CHARACTERISTICS* and the *AC ELECTRICAL CHARACTERISTICS* sections of this data sheet). However, when the DS18B20 is performing temperature conversions or copying data from the scratchpad memory to EEPROM, the operating current can be as high as 1.5mA. This current can cause an unacceptable voltage drop across the weak 1-Wire pullup resistor and is more current than can be supplied by C_{PP}. To assure that the DS18B20 has sufficient supply current, it is necessary to provide a strong pullup on the 1-Wire bus whenever temperature conversions are taking place or data is being copied from the scratchpad to EEPROM. This can be accomplished by using a MOSFET to pull the bus directly to the rail as shown in Figure 4. The 1-Wire bus must be switched to the strong pullup within 10μs (max) after a Convert T [44h] or Copy Scratchpad [48h] command is issued, and the bus must be held high by the pullup for the duration of the conversion (t_{conv}) or data transfer (t_{WR} = 10ms). No other activity can take place on the 1-Wire bus while the pullup is enabled.

The DS18B20 can also be powered by the conventional method of connecting an external power supply to the V_{DD} pin, as shown in Figure 5. The advantage of this method is that the MOSFET pullup is not required, and the 1-Wire bus is free to carry other traffic during the temperature conversion time.

OPERATION — MEASURING TEMPERATURE

The core functionality of the DS18B20 is its direct-to-digital temperature sensor. The resolution of the temperature sensor is user-configurable to 9, 10, 11, or 12 bits, corresponding to increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively. The default resolution at power-up is 12-bit. The DS18B20 powers-up in a low-power idle state; to initiate a temperature measurement and A-to-D conversion, the master must issue a Convert T [44h] command. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the DS18B20 returns to its idle state. If the DS18B20 is powered by an external supply, the master can issue "read time slots" (see the *1-WIRE BUS SYSTEM* section) after the Convert T command and the DS18B20 will respond by transmitting 0 while the temperature conversion is in progress and 1 when the conversion is done. If the DS18B20 is powered with parasite power, this notification technique cannot be used since the bus must be pulled high by a strong pullup during the entire temperature conversion. The bus requirements for parasite power are explained in detail in the *POWERING THE DS18B20* section of this datasheet.

The DS18B20 output temperature data is calibrated in degrees centigrade; for Fahrenheit applications, a lookup table or conversion routine must be used. The temperature data is stored as a 16-bit sign-extended two's complement number in the temperature register (see Figure 2). The sign bits (S) indicate if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. If the DS18B20 is configured for 12-bit resolution, all bits in the temperature register will contain valid data. For 11-bit resolution, bit 0 is undefined. For 10-bit resolution, bits 1 and 0 are undefined, and for 9-bit resolution bits 2, 1 and 0 are undefined. Table 2 gives examples of digital output data and the corresponding temperature reading for 12-bit resolution conversions.

TEMPERATURE REGISTER FORMAT Figure 2

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LS Byte	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
	bit 15	**bit 14**	**bit 13**	**bit 12**	**bit 11**	**bit 10**	**bit 9**	**bit 8**
MS Byte	S	S	S	S	S	2^6	2^5	2^4

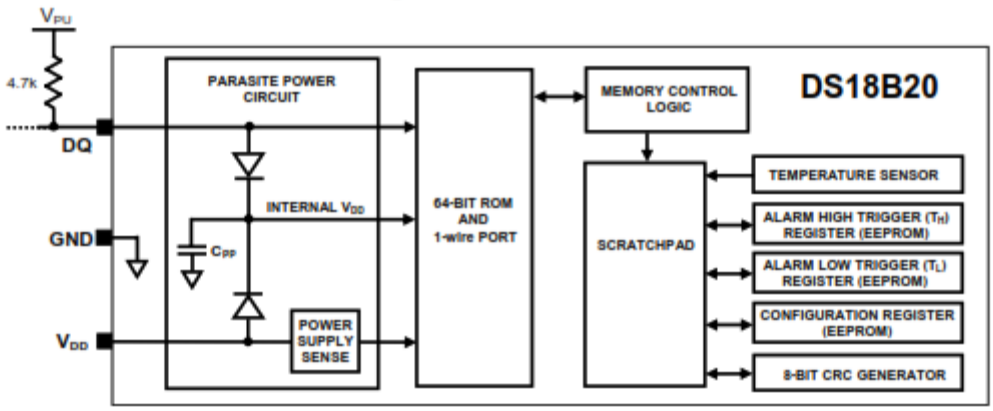
TEMPERATURE/DATA RELATIONSHIP Table 2

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	0000 0111 1101 0000	07D0h
+85°C*	0000 0101 0101 0000	0550h
+25.0625°C	0000 0001 1001 0001	0191h
+10.125°C	0000 0000 1010 0010	00A2h
+0.5°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h
-0.5°C	1111 1111 1111 1000	FFF8h
-10.125°C	1111 1111 0101 1110	FF5Eh
-25.0625°C	1111 1110 0110 1111	FE6Fh
-55°C	1111 1100 1001 0000	FC90h

*The power-on reset value of the temperature register is +85°C

Another feature of the DS18B20 is the ability to operate without an external power supply. Power is instead supplied through the 1-Wire pullup resistor via the DQ pin when the bus is high. The high bus signal also charges an internal capacitor (C_{PP}), which then supplies power to the device when the bus is low. This method of deriving power from the 1-Wire bus is referred to as "parasite power." As an alternative, the DS18B20 may also be powered by an external supply on V_{DD}.

DS18B20 BLOCK DIAGRAM Figure 1



ORDER INFORMATION

ORDERING NUMBER	PACKAGE MARKING	DESCRIPTION
DS18B20	18B20	DS18B20 in 3-pin TO92
DS18B20/T&R	18B20	DS18B20 in 3-pin TO92, 2000 Piece Tape-and-Reel
DS18B20+	18B20 (See Note)	DS18B20 in Lead-Free 3-pin TO92
DS18B20+T&R	18B20 (See Note)	DS18B20 in Lead-Free 3-pin TO92, 2000 Piece Tape-and-Reel
DS18B20U	18B20	DS18B20 in 8-pin uSOP
DS18B20U/T&R	18B20	DS18B20 in 8-pin uSOP, 3000 Piece Tape-and-Reel
DS18B20U+	18B20 (See Note)	DS18B20 in Lead-Free 8-pin uSOP
DS18B20U+T&R	18B20 (See Note)	DS18B20 in Lead-Free 8-pin uSOP, 3000 Piece Tape-and-Reel
DS18B20Z	DS18B20	DS18B20 in 150 mil 8-pin SO
DS18B20Z/T&R	DS18B20	DS18B20 in 150 mil 8-pin SO, 2500 Piece Tape-and-Reel
DS18B20Z+	DS18B20 (See Note)	DS18B20 in Lead-Free 150 mil 8-pin SO
DS18B20Z+T&R	DS18B20 (See Note)	DS18B20 in Lead-Free 150 mil 8-pin SO, 2500 Piece Tape-and-Reel

Note: A "+" symbol will also be marked on the package.

DETAILED PIN DESCRIPTIONS Table 1

SO*	µSOP*	TO-92	SYMBOL	DESCRIPTION
5	4	1	GND	**Ground.**
4	1	2	DQ	**Data Input/Output pin.** Open-drain 1-Wire interface pin. Also provides power to the device when used in parasite power mode (see "Parasite Power" section.)
3	8	3	V_{DD}	**Optional V_{DD} pin.** V_{DD} must be grounded for operation in parasite power mode.

*All pins not specified in this table are "No Connect" pins.

OVERVIEW

Figure 1 shows a block diagram of the DS18B20, and pin descriptions are given in Table 1. The 64-bit ROM stores the device's unique serial code. The scratchpad memory contains the 2-byte temperature register that stores the digital output from the temperature sensor. In addition, the scratchpad provides access to the 1-byte upper and lower alarm trigger registers (T_H and T_L), and the 1-byte configuration register. The configuration register allows the user to set the resolution of the temperature-to-digital conversion to 9, 10, 11, or 12 bits. The T_H, T_L and configuration registers are nonvolatile (EEPROM), so they will retain data when the device is powered down.

The DS18B20 uses Dallas' exclusive 1-Wire bus protocol that implements bus communication using one control signal. The control line requires a weak pullup resistor since all devices are linked to the bus via a 3-state or open-drain port (the DQ pin in the case of the DS18B20). In this bus system, the microprocessor (the master device) identifies and addresses devices on the bus using each device's unique 64-bit code. Because each device has a unique code, the number of devices that can be addressed on one bus is virtually unlimited. The 1-Wire bus protocol, including detailed explanations of the commands and "time slots," is covered in the *1-WIRE BUS SYSTEM* section of this datasheet.

DALLAS SEMICONDUCTOR MAXIM

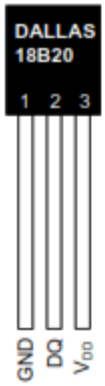
DS18B20
Programmable Resolution 1-Wire Digital Thermometer

www.maxim-ic.com

FEATURES

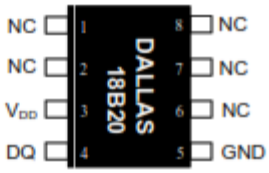
- Unique 1-Wire® interface requires only one port pin for communication
- Each device has a unique 64-bit serial code stored in an onboard ROM
- Multidrop capability simplifies distributed temperature sensing applications
- Requires no external components
- Can be powered from data line. Power supply range is 3.0V to 5.5V
- Measures temperatures from –55°C to +125°C (–67°F to +257°F)
- ±0.5°C accuracy from –10°C to +85°C
- Thermometer resolution is user-selectable from 9 to 12 bits
- Converts temperature to 12-bit digital word in 750ms (max.)
- User-definable nonvolatile (NV) alarm settings
- Alarm search command identifies and addresses devices whose temperature is outside of programmed limits (temperature alarm condition)
- Available in 8-pin SO (150mil), 8-pin µSOP, and 3-pin TO-92 packages
- Software compatible with the DS1822
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system

PIN ASSIGNMENT

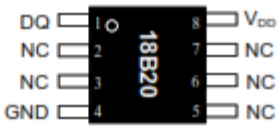


(BOTTOM VIEW)

TO-92
(DS18B20)



8-Pin 150mil SO
(DS18B20Z)



8-Pin µSOP
(DS18B20U)

PIN DESCRIPTION

GND - Ground
DQ - Data In/Out
V_{DD} - Power Supply Voltage
NC - No Connect

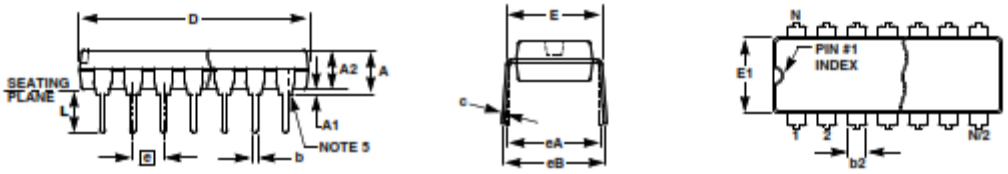
DESCRIPTION

The DS18B20 Digital Thermometer provides 9 to 12–bit centigrade temperature measurements and has an alarm function with nonvolatile user-programmable upper and lower trigger points. The DS18B20 communicates over a 1-Wire bus that by definition requires only one data line (and ground) for communication with a central microprocessor. It has an operating temperature range of –55°C to +125°C and is accurate to ±0.5°C over the range of –10°C to +85°C. In addition, the DS18B20 can derive power directly from the data line ("parasite power"), eliminating the need for an external power supply.

Each DS18B20 has a unique 64-bit serial code, which allows multiple DS18B20s to function on the same 1–wire bus; thus, it is simple to use one microprocessor to control many DS18B20s distributed over a large area. Applications that can benefit from this feature include HVAC environmental controls, temperature monitoring systems inside buildings, equipment or machinery, and process monitoring and control systems.

1-Wire is a registered trademark of Dallas Semiconductor.

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

NOTES:

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

BIODATA PENULIS

Penulis buku tesis dengan judul “Sistem Pengisian Baterai Nirkabel dengan Panel Surya Menggunakan Metode Fuzzy” ini bernama Alfarid Hendro Yuwono. Penulis dilahirkan di Surabaya, 2 Mei 1990, anak dari pasangan Yatno Yuwono. Rekam pendidikan formal penulis dimulai dari SDN Banyu Urip VIII Surabaya (1997-2003), SMPN 3 Surabaya (2003-2006), dan SMAN 6 Surabaya (2006-2009). Pada masa Sekolah Dasar, penulis jatuh hati pada mata pelajaran IPA, khususnya saat mengerjakan tugas prakarya rangkaian listrik sederhana, sehingga pada tahun 2009 penulis mulai menempuh pendidikan tinggi di program studi D4 Teknik Elektronika PENS-ITS dan berhasil lulus pada tahun 2014. Kemudian penulis mengabdi di Surau Nurul Amin Surabaya hingga tahun 2016. Selanjutnya, karena kecintaannya pada dunia pendidikan, pada tahun 2016 penulis melanjutkan studinya di program magister jurusan Teknik Elektro, bidang keahlian Elektronika, Institut Teknologi Sepuluh Nopember. Selama masa perkuliahan, penulis berkesempatan untuk mengikuti berbagai macam kegiatan seminar nasional dan internasional. Penulis hanyalah hamba Alloh SWT yang tidak luput dari salah dan dosa.